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SIMPLE HIGH PERFORMANCE GENERAL PURPOSE SINGLE CHANNEL ANALYSER

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Abstract

A simple single channel analyser using standard components is described. High temperature stability (0.002% / °C) and resolution (≃ 100 μV) is achieved. The two-level generator circuits described allow full DC coupling of the input pulses. The performance of these circuits is discussed in detail and experimental results presented.

Introduction

The development of inexpensive linear integrated circuits has made it worth the rethinking of the working principles of nuclear electronics equipment. Circuits that are at the same time simpler, cheaper and have superior performance can, in principle, be developed. With these ideas in mind, and noticing that the stability and trigger precision of commercial single channel analysers seldom reach figures compatible with the ones of linear pulse amplifiers, we decided to exploit the possibility of having improved performance through the use of standard components like operational amplifiers, comparators and zener diodes. In the present work we describe two alternative circuits for single channel analysers and discuss their performances.

DC two-level generator circuits

The upper and lower DC voltage levels required to define the window of a single channel analyser were generated by circuits that, unlike the ones of most commercial units (e.g. ORTEC 420A, H.P. 5583) which only allow AC coupling, allow full DC coupling of the pulses to be analysed.

Two alternative DC levels generator circuits are shown in a schematic way in Figs. 1 and 2. In both circuits the window width ΔE is constant and independent on the base line voltage, E.

In the first one (Fig. 1) E is derived from a potentiometer, R_1, in parallel with a zener diode, Z_1, which is fed through a resistor R_0. This DC level is available at the output of operational amplifier A_1, connected as a voltage follower. ΔE is generated across potentiometer R_2 in parallel with zener Z_2 which is fed by a current source I_1. This voltage is added to E in the way shown and $E + \Delta E$ is available at the output of operational amplifier A_2. The use of high impedance sources to feed the zeners allow high temperature stability if the bias current intensity is set for the value (I_{ZT}) given by the manufacturer. Current source I_2 ($\simeq I_1$) doesn't need to be a high performance one, since it is used only to sink I_1, thus protecting the output of operational amplifier A_1.

The second circuit it is shown in Fig. 2 and uses the same basic components as the first one but in a different arrangement: operational amplifier A_2 is in the feedback loop of A_1, and the ΔE generator circuit in the loop of A_2. Now, E is obtained at the output of A_2 and $E + \Delta E$ at the output of A_1.

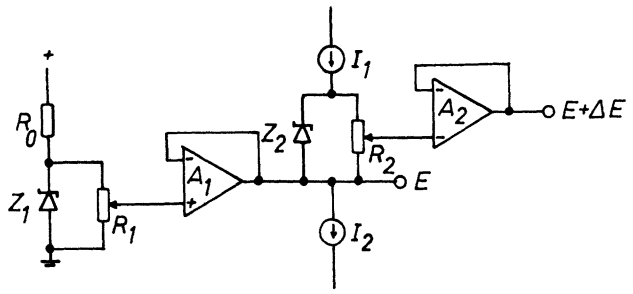

Fig. 1 — DC level generator circuit: first configuration

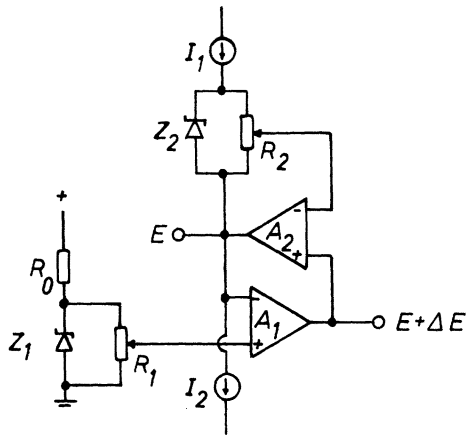

Fig. 2 — DC level generator circuit: second configuration

The importance of the input offset voltage and bias currents of the operational amplifiers in the performance of the circuits of Figs. 1 and 2 can be discussed with the help of Figs. 3 and 4, respectively. In these Figures R_1' and R_2' are the internal resistances for the Thévenin equivalent circuit for the generators of the voltages E and ΔE, e_{os1} and e_{os2} are the offset voltages of A_1 and A_2, respectively, and I_{1+}, I_{1-}, I_{2+} and I_{2-} the input bias currents for the operational amplifiers.

To reduce the input current errors the compensation resistances R_{c1} and R_{c2}, in Figs. 3 and 4, are made equal to R_1' and R_2' respectively. In practice since the values of R_1' and R_2' depend on the setting of the potentiometers R_1 and R_2 of Figs. 1 and 2, the actual values to be taken are those for an average setting, i.e. $R_{c1} \simeq R_1 / 4$ and $R_{c2} \simeq R_2 / 4$. If the input offset currents for the operational amplifiers A_1 and A_2 are $I_{01} \equiv I_{1+} - I_{1-}$ and $I_{02} \equiv I_{2+} - I_{2-}$, respectively, we can write for the output voltages of the circuit of Fig. 3:

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$$V_2 = E + e_{os1} + R_1' I_{01}$$

$$V_1 = E + \Delta E + e_{os1} + e_{os2} + R_1' I_{01} + R_2' I_{02}$$

and for the circuit of Fig. 4

$$V_2 = E + e_{os1} + R_1' I_{01}$$

$$V_1 = E + \Delta E + e_{os1} - e_{os2} + R_1' I_{01} - R_2' I_{02}$$

These results show that, since the offset voltages and currents are only given in absolute values, the actual deviations from the exact values E and E + ΔE, are the same for both circuits.

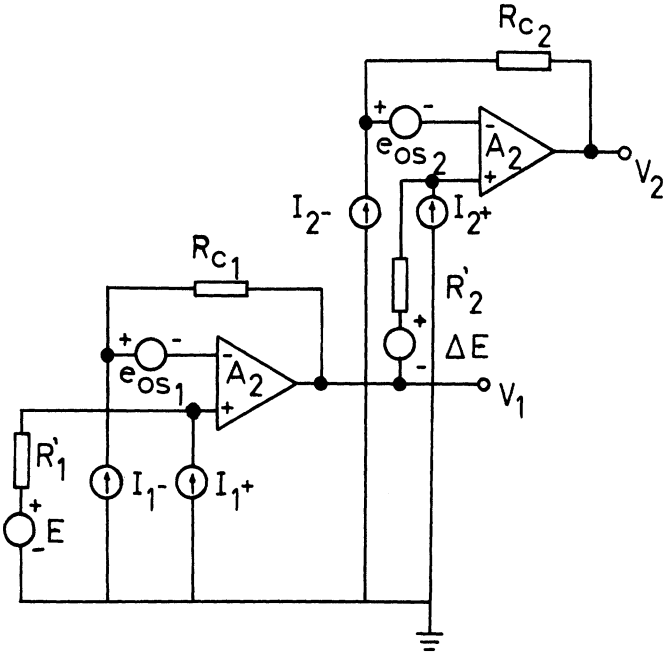

Fig. 3 — First configuration equivalent circuit

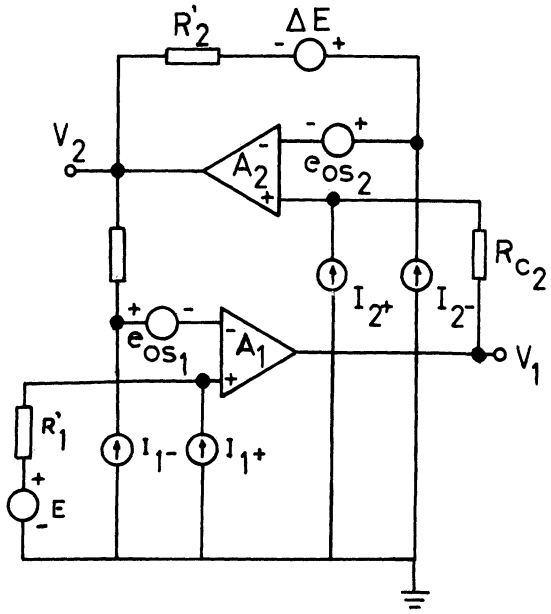

Fig. 4 — Second configuration equivalent circuit

The single-channel analyser circuits

In Fig. 5 it is shown the actual circuit for the version of the single-channel analyser based on a DC level generator of the type of Fig. 1. The other version, not shown, it is quite similar to this one apart from the features that distinguish the circuit of Fig. 2 from the one of Fig. 1. The single-channel analyser circuit uses only NIM power supplies (+24 V, 100 mA; +12 V, 100 mA; -12 V, 50 mA). Current source I_1 (refer to Fig. 1), has a good temperature stability and it is built around operational amplifier A_3 (301 A type), high gain 2N3638A transistor and zener Z_3. The calculated temperature coefficient using a 1N829 zener it is better than 0.2 μA/°C for a current of 8 mA.

A simple current source based on transistor BFY 50 it is used for I_2. The two networks for offset compensation of operational amplifiers A_1 and A_2 are based on transistors 2N2905 in a standard configuration which minimizes the offset drift. A switch before A_1, allows the use of an external baseline voltage (E_{ext}).

The voltage comparison circuits C_0, C_1 and C_2 are based on dual 711 comparators with capacitive positive feedback to achieve high triggering precision, in a configuration described by BAYER[1]. Zeners Z_4 to Z_9 are used to give independent +12 V and -6 V supplies for the comparators. The comparison voltages for C_0, C_1 and C_2 are set for the near zero (≃ 50 mV), E and E + ΔE levels, respectively. As the maximum input differential voltage for the 711's is 5 Volts, the input pulse amplitudes is reduced to half with two 1 kΩ resistors. The two 1.5 kΩ resistors before the negative inputs of C_1 and C_2 allow compensation for the input bias currents. The networks around the 2N2905 transistors and the 220 kΩ potentiometers are for offset adjustment. Since the 711's haven't got offset control, zero offset for the $A_1 - C_1$ and the $A_2 - C_2$ systems is achieved through the offset adjustment of the respective operational amplifier, using a method to be described in future work.

The logic circuitry is standard and based on a 7473 flip-flop and two single-shots fed by the output of C_1 and built with two-input NAND gates (7400). The flip-flop, which is normally reset, is set by an input pulse exceeding the E + ΔE level and thus the single-shot output is inhibited through the Q output, when the trailing edge of the pulse crosses the E level; for pulses between E and E + ΔE that output it is not inhibited and an output pulses arises. The second single-shot it is always triggered at the same time than the first one and, after a small delay introduced by an RC integrator between two inverters, the flip-flop is reseted.

The near zero level comparator, C_0, is available for timing and can be used, in principle, for pile-up rejection logic circuitry.

Experimental results and discussion

The differential non-linearity was estimated at the DC level generators outputs, by measuring the variation of ΔE (using a floating input DVM) as a function of the base line voltage E. It was found to be less than 10 μV for channel widths of the order of 10 - 100 mV, and 20 μV for widths of around 1 mV, for both configurations of the single-channel analyser.

The integral linearity was measured by a method to be described in future work using an ORTEC 448 precision pulse generator and a ramp voltage. The difference between the DC level E and the pulse amplitude necessary to trigger the comparator was measured as a function of E. The integral non-linearity was found to be less than 0.01 % for the two configurations.

The trigger precision (resolution) for descrimination, which is defined as the half-width of the derivative of the function that gives the probability of triggering the discriminator (comparator output) as a function of the input pulse amplitude, is 100 μV.

The temperature coefficients of the DC level generators measured at the points E and E + ΔE (Fig. 5) was measured to be better than 0.0015 and 0.003 % / °C, respectively, for the temperature range of 25 to 80 °C.

These experimental results show that the two versions of single-channel analysers have very similar performances. They allow precision single channel pulse amplitude measurements.

Acknowledgments

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Reference

1 - R. BAYER, Electronics, 46, nº 25(Dec. 6, 1975), 114.

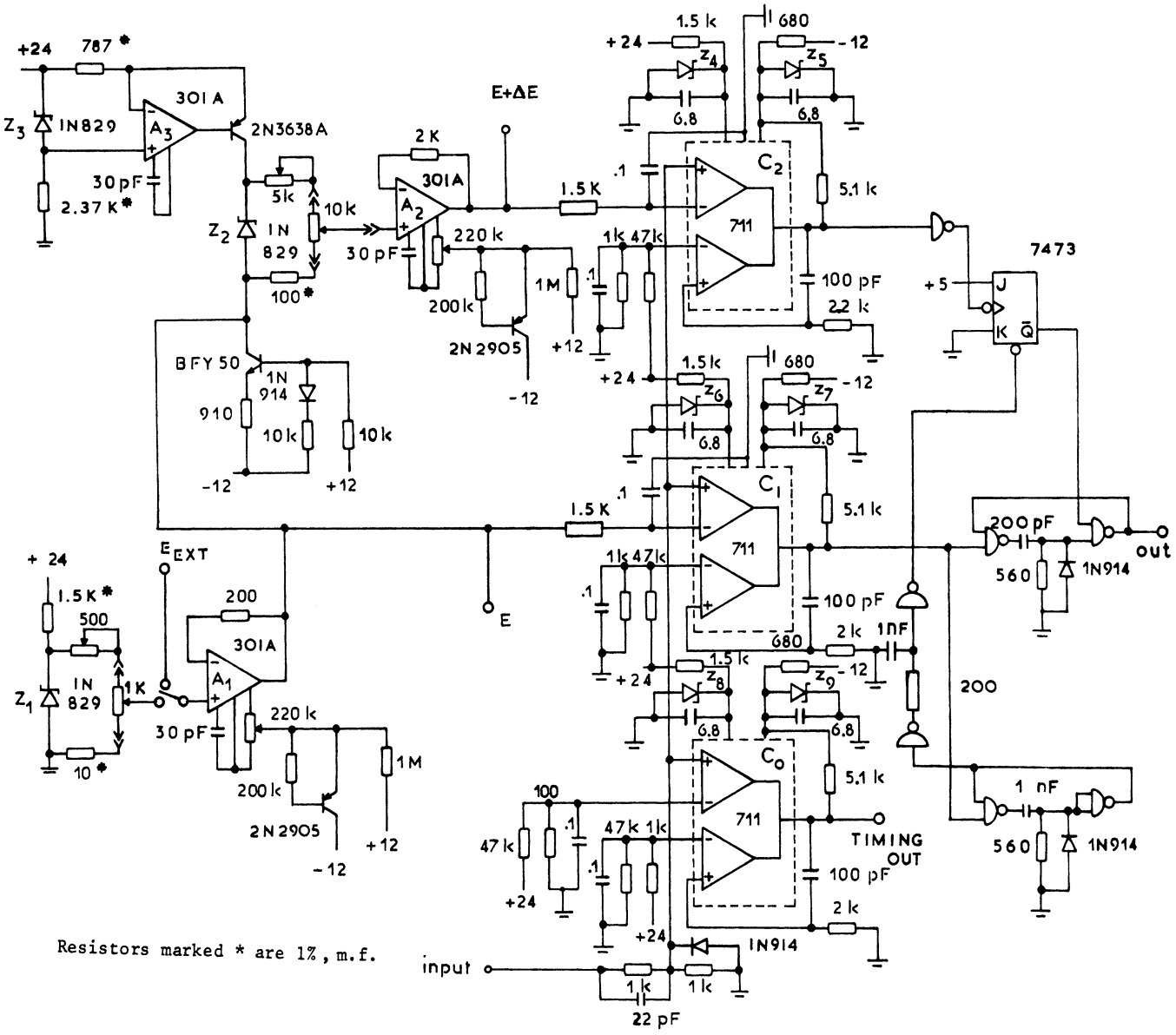

Fig. 5 —
Complete circuit for the first configuration of the single-channel analyser