IEEE Transactions on Nuclear Science, Vol. NS-29, No. 1, February 1982

SMALL SIZE, LOW COST MULTICHANNEL ANALYZER BASED ON AN SDK 85 WITH THE A/D CONVERSION AND DATA ACQUISITION FUNCTIONS IMPLEMENTED BY SOFTWARE

F.A.F. Fraga
Physics Department, University of Coimbra,
3000 Coimbra, Portugal

Summary

We describe a small size low cost 128-256 channels multichannel analyser based on an SDK85 microcomputer board using a minimum of external low cost circuitry. This circuitry consists only of a quad comparator, three operational amplifiers and three integrated analog switches and very few discrete components. The pulse amplitude conversion is carried out fully by software. This software as well as that for data acquisition and output functions is described and results are presented.

In fields like environ mental, biological, nuclear, medical or educational instrumentation there is a need for small size, low cost portable multichannel analysers. Performances like 500μs mean deadtime and 256 channels are more than sufficient for manny applications where channel resolution and count speed are limited by the experimental situation. Recently, systems using microprocessor techniques have been described[1]. However, as the microprocessor is used mainly for digital data organization and display, an ADC and a good deal of analog logic circuitry, such as DMA controlers, storage registers, logic gating systems, etc. are required. These systems can have a large number of channels, but their cost is relatively high. For those applications where a smaller number of channels and counting rates up to a few thousand per second are sufficient the cost of the multichannel analyser can be substantially reduced if the ADC's and external logic functions are fully carried out by software and the circuits for the analog functions are reduced to a minimum using standard low cost components.

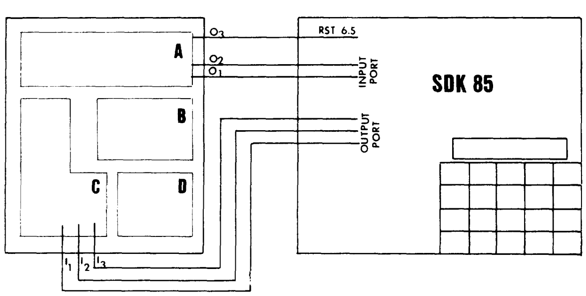

Fig.1 Analog board connected to the SDK85.

We have developed such a multichannel analyser built around an SDK85 Intel kit which uses an 8085 microprocessor chip. The general philosophy of our design can be implemented with almost any other 8 bit microprocessor, and improvements can be added if faster microprocessors are used. The system was built and tested with 128 channels but can be easily expanded with small software changes to 256 or even 512 channels. The hardware diagrams are shown in Fig. 1 and Fig. 2. The SDK85 microcomputer is shown in Fig. 1 with the analog signal circuit connected to the I/O ports.

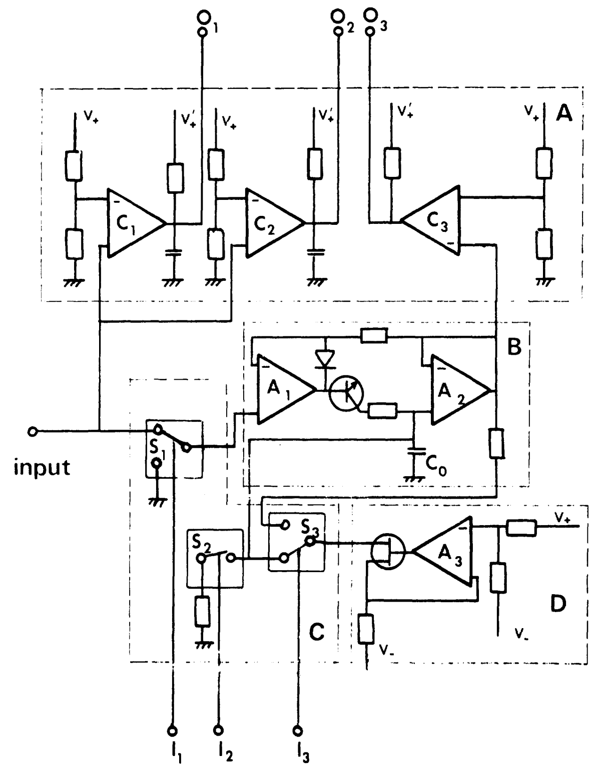

Fig. 2 Analog circuit diagram. Only seven I.C.'s a transistor, a FET and a few resistors are used.

Output lines to control the dispaly DAC's and the six input lines needed to use an optional external keyboard are not shown. All input--output signals of the analog circuit are TTL compatible so that the board is directly connected to the SDK85. The analog circuit is shown in more detail in Fig. 2 and besides the two ADC's for X-Y output it is the only cir-

0018-9499/82/0200-0129$00.75©1982 IEEE

cuitry external to the SDK85.

This circuit is implemented with only six standard low cost integrated circuits, all easily available, one FET and a few resistors. The integrated circuits are non critical and and can be replaced by similar CMOS devices

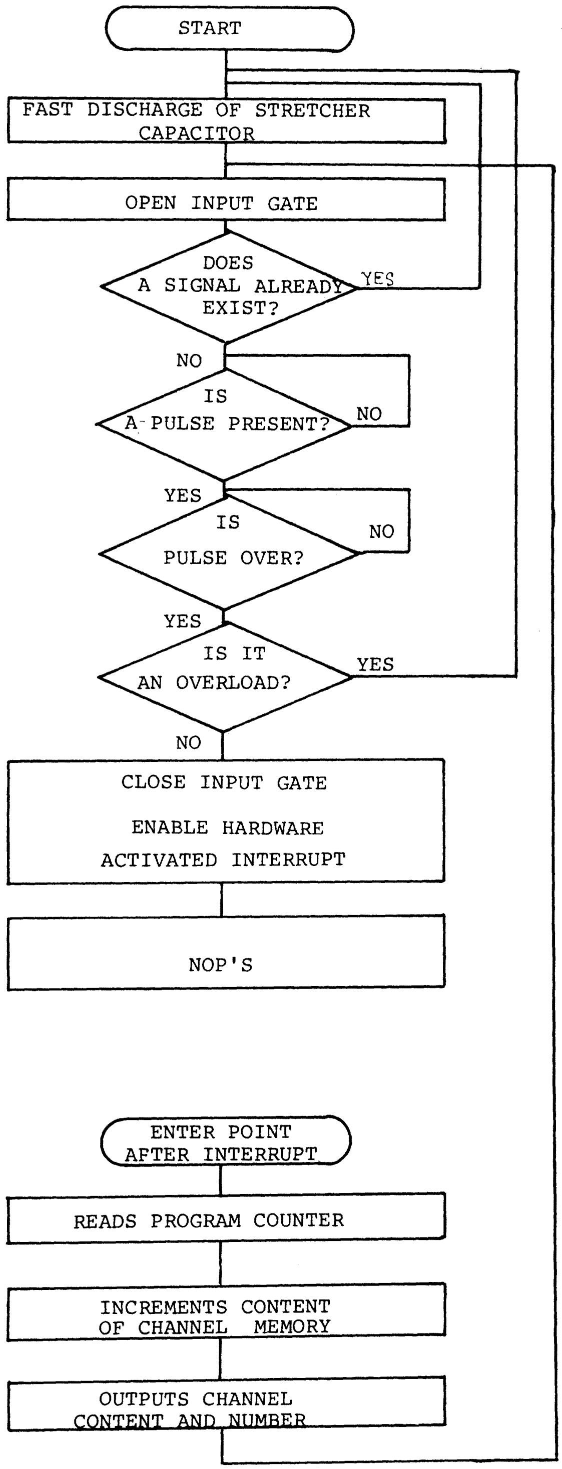

Fig. 3 Main program flowchart.

reducing power consumption to a few mW. Block A is the comparator, B the stretcher, C the analog gates and D the constant current source.

Block A is built around a single inexpensive LM339 quad comparator. The pull-up output resistors are connected to the +5V supply so that TTL compatible outputs are generated. The increase in rise time due to the the use of this lower voltage is of no practical consequence and allows direct connection to the ports. The value of the output capacitance is such that the delay in the high to low transition is of the order of the microprocessor test period of that input line in order to guarantee that the microprocessor never misses the outputs of the two comparators.

The stretcher configuration is a common one. The values of resistors and C_o can be tailored to suit the shape of the input signal. However slow, this stretcher is good enough for most applications. The gating block C was built with Texas Instruments TL 601 and TL610 integrated linear gates. Its transient and comuting performances were found to be accurate enough. Because of the non availability of an integrated current source with good transient performance, an operational amplifier and a FET were used to linearly discharge the stretcher capacitor. The use of a double pole switch S_3 reduces transient charge transfers during switching.

Fig. 3 is the flowchart of the main program. To be ready to accept pulses the microprocessor turns on S_2 quickly discharging C_o. Afterwards it connects the input signal to the stretcher and makes a test to C_1 output. If an input signal already exists the program is reinitialized and the signal is rejected to avoid conversion errors. If not the microprocessor tests the output of C_1 waiting until a pulse arrives. Then it waits until the pulse has decayed and checks for overloading, testing the output of C_2. If at any moment the signal exceeds the overload level the pulse is ignored and the program reinitialized. Otherwise S_1 is turned off, the hardware interrupt enabled and S_3 connects C_2 to the linear current source. After this, the microprocessor executes a number of "no operation" instructions that depends on the pulse amplitude, until an interrupt occurs. Then the digital value of the amplitude of the pulse is extracted from the content of the program counter which is proportional to the discharge time. This technique gives an improvement on the counting speed over conventional iterative algoritms because jump instructions are avoided and the "no operation" instruction is faster than the "increment" one. After the interrupt the cell memory corresponding to that channel number is incremented, the microprocessor outputs the content and number of the channel to the X-Y DAC's and it is ready for a new conversion cycle. If the live display feature is unnecessary the output instructions can be omitted.

Subroutines for CRT display, plotter, LED display, channel sellection and printer were developed and successfully used. A fully software supported keyboard was equally incorporated in the prototype.

The measured differential linearity, for pulses with risetime about 1μs was about 1% and was limited by the stretcher. Average deadtime was about 200μs. Fig. 4 shows a typical spectrum obtained with a ^{60}Co source. The counting rate was about 2000 pulses per second.

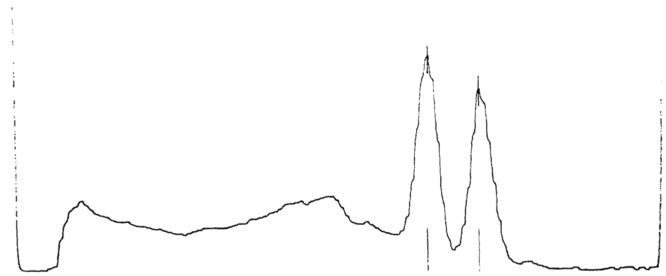

Fig. 4 Spectrum obtained from a ^{60}Co source using a NaI(II) detector.

ACKNOWLEDGEMENTS

This work has been supported by INIC under Research Project CF/2.

The author wishes to thank C.A.N. Conde and C.A.B. Correia for valuable discussions and suggestions.

References

1 - M.A. WOLF and C.J. UMBARGER, IEEE Trans. Nucl. Sci. NS-27 (1980) 322.