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Enhanced neutron diagnostics data acquisition system based on a time digitizer and transient recorder hybrid module

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Abstract

This paper proposes a new transient recorder (TR)–time digitizer (TD) hybrid system to be used to pull out higher performance of presently used techniques for measuring the collimated flux and the spectrum of the neutron emission from fusion plasmas of either deuterium or deuterium–tritium, as well as to apply to new neutron measuring techniques, with demanding specific requirements in plasma physics. This system is presented as a modular design, allowing up to four 200 MHz, 12 b acquisition channels to operate in an interleaved way, achieving 800 MHz. The module includes a XILINX FPGA and an ADC front-end along with a large memory storage capacity and unique TD capabilities (two channels with 36 ps resolution). The FPGA is able to perform real-time data validation as well as some processing algorithms to obtain physical parameters and module calibration. Processed data will be transferred to a control unit by a gigabit optical link. The system will be able to support multiple front-end modules operating synchronously.

Keywords: Data acquisition; Neutron diagnostics; Transient recorder; Time digitizer; ADC interleaved architecture; Real-time systems; Signal processing

1. Introduction

Neutron diagnostics (ND) play an important role in plasma physics as neutron emission is an important carrier of information about the state of fusion plasmas. ND at JET[1] include: (i) total neutron yield rate, $Y_n(t)$, provided by flux detectors which do not differentiate between neutrons of different energies and are calibrated relative to certain standards and model computation (i.e., not absolute); (ii) neutron profile data from neutron cameras; (iii) energy distribution of collimated neutron flux by neutron emission spectroscopy (NES). NES presents visible enhancements over the

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past 10 years, for instance, the upgrade magnetic proton recoil (MPRu) and the time of flight optimized rate spectrometers [1–3].

Motivated by ITER[2] needs, further improvements on neutron diagnostics capabilities at JET are being considered. The aim is to have absolute measurement of $Y_n(t)$ at high count rate and 2.5 MeV neutrons identification in either D or DT reacting plasmas. With this purpose, a system named MPR-F combining MPRu spectrometer and flux detectors is being designed in order to have neutron spectrum and flux measurements with improved time resolution over large dynamic range [4]. Regarding flux detectors, there are two major issues to solve, setting the threshold, which defines the minimum energy of neutrons that will be accepted in the data and separation of neutrons from background of extraneous radiation, e.g., neutron/gamma discrimination. For the spectrometers the figure of merit is the count rate, leading to fast and continuous acquisition modules.

A new data acquisition system based on TR–TD hybrid module is being developed with the following characteristics: (i) Amplitude resolution of 10–12 b to cope with the expected signal-to-noise ratio (SNR) of the input pulses; (ii) sampling rate of 50 Msamples/s to 2 GSPS for accurate pulse shaping; (iii) 1 GB of local memory sufficient to store the pulses at the expected rate, during the experiment duration (seconds or tens of seconds).

2. System description

This enhanced ND system is presented as a modular TR–TD data acquisition design optically linked to its control unit, in order to be positioned near the diagnostic (Fig. 1). The MPR-F diagnostic requires at least five of these acquisition modules (20 channels) to be implemented on flux detectors in the 19 channels of the JET neutron cameras.

These TR–TD data acquisition modules are plugged into a controller unit through a gigabit communication link as a substitute for the usual PCI[3] or VME[4] parallel busses.

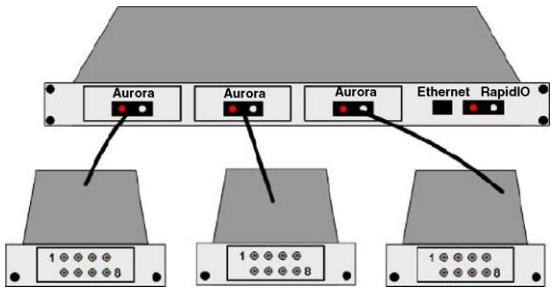

Fig. 1. Enhanced neutron diagnostics hybrid data acquisition system.

The controller module is based on a low power system-on-chip, which includes two PowerPC processors, 512 MB of memory, 8 Gb links and 10/100 Mb Ethernet. The case is a standard 19 in. 2U box with miniITX power supply and forced air ventilation. The operating system will be the LGPL[5] licensed PowerPC Linux with RTAI[6] extensions ported to this specific hardware platform. The controller unit will have interconnection to CODAS[7] through an Ethernet port. RapidIO interface is also provided for real-time data moving and system monitoring.

Next sections will describe in more detail the TR–TD module.

2.1. Module architecture

The TR–TD module is based on FPGA (XCV2P30 from XILINX^{TM}) allowing three acquisition architectures, configurable by software: (i) four analogue channels at 200 MSPS; (ii) two channels at 400 MSPS based on two interleaved ADCs; (iii) one channel at 800 MSPS based on four interleaved ADCs.

Fig. 2 describes the module architecture with four hybrid input channels featuring 12 b resolution at 200 MHz sampling rate, for the TR function and 72 ps resolution in a single-chip time to digital converter, achieving 37 ps operating with only two channels. This TD capability permits high accuracy time and amplitude measurements in applications where correlation between both parameters is essential like time-of-flight measurements or coincident trigger discrimination.

[2] "The way" in Latin.
[3] Peripheral component interconnect.
[4] VERSAmodule Eurocard.
[5] The GNU lesser general public license.
[6] Real-time application interface.
[7] Code ocean data analysis system.

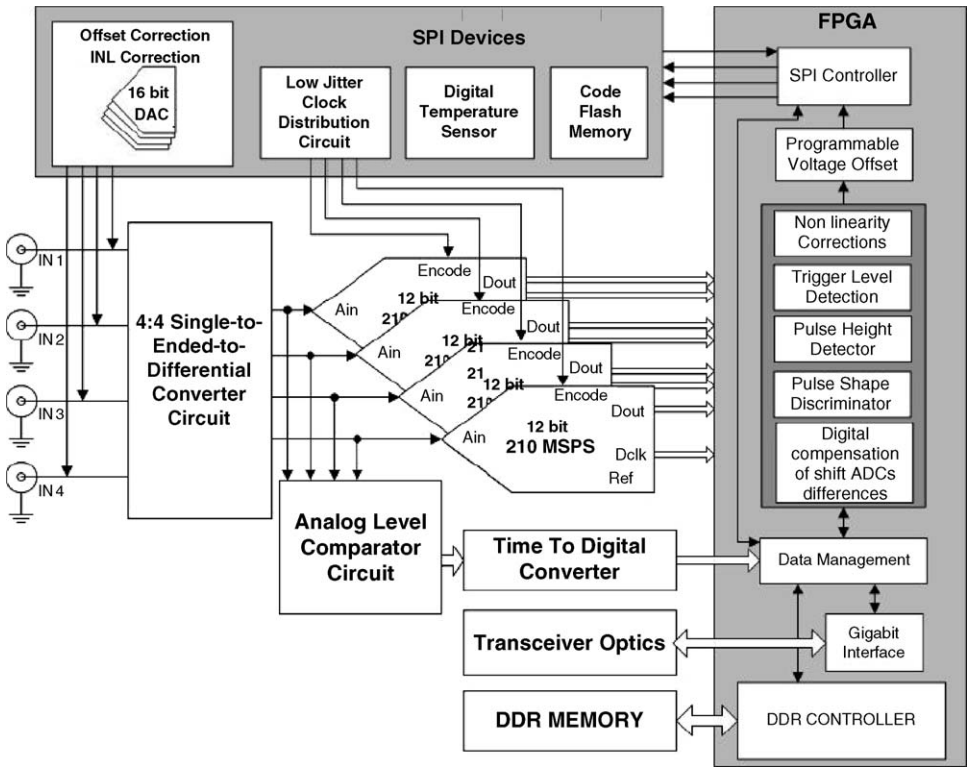

Fig. 2. TR–TD module block diagram.

The FPGA directly connected to the free-running ADC channels performs the following main tasks: (i) analogue inputs calibration; (ii) data storage management; (iii) 3.125 Gb communications interface; (iv) data processing, including data reduction by pulse height analysis and pulse shape discrimination; (v) complex managing modes of triggering (auto-triggering functionality) and finally (vi) serial peripheral interface (SPI) controller. The module provides 1 GB of double data rate (DDR) synchronous dynamic random access memory.

Interleaved architectures, where channels mismatches are crucial, need temperature sensors to permit calibration of several temperature dependent parameters.

2.2. Interleaved architecture

At present, the fastest commercially available 12 b analogue to digital converter (ADC) is the AD9430, from analogue devices®, which is rated to run at 210 MSPS. Faster 12 b ADCs can be achieved with the already mentioned interleaved architectures, although it represents an immediate threat to the 11 b dynamic range performance (68 dB).

At a performance level of 10 b and above, in interleaved architecture, the dynamic range is dependent on the gain, phase and offset matching between each individual ADC channel. For interleaving mode the following must be noted: (i) the same signal must be attached to each of the 50 Ω input channel connectors of the corresponding interleaved ADCs, the inherent gain mismatches are digitally compensated; (ii) each ADC has its own internal voltage reference. The possible resultant difference between ADC offsets can be corrected, during module calibration stage, by a 16 b, quad voltage output digital-to-analogue converter; (iii) all ADCs sample at 200 MHz, giving an overall data rate of 400 MHz for two channels, with each clock phased at 180° intervals and 800 MHz for one channel, with each clock phased at 90° intervals.

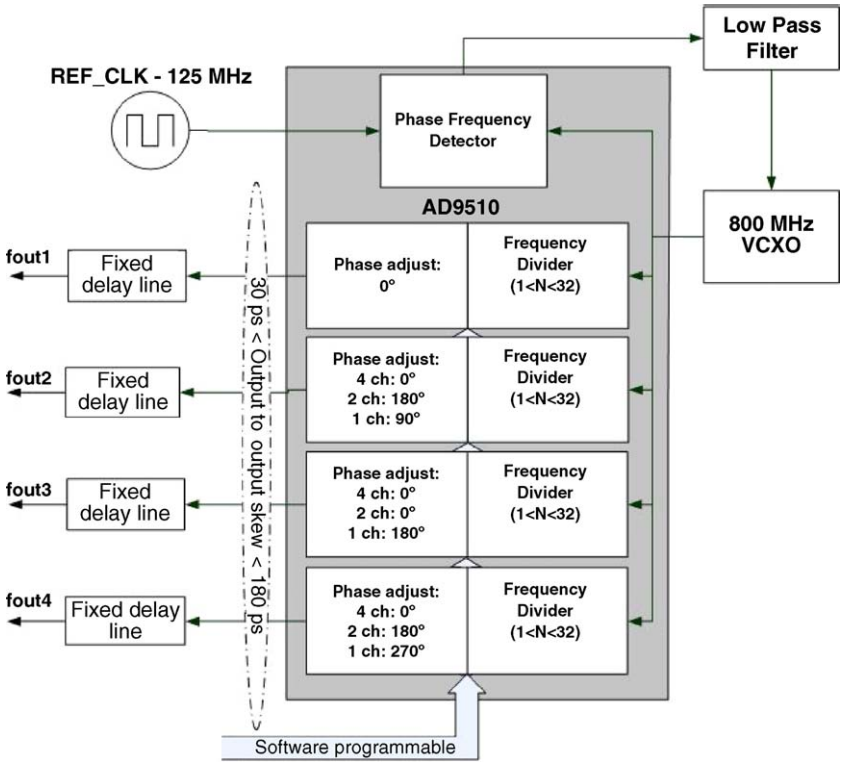

Fig. 3. 800 MHz distribution circuit and clock synthesis.

As ADCs dynamic performance decreases with clock jitter, for this architecture a high quality clock with a maximum rms jitter of 634 fs is needed [5]. Fig. 3 presents the clock distribution circuit exhibiting 355 fs rms jitter (simulated). Fixed delay adjusts were used at each output to fix the clock synthesizer output skew variation (30–180 ps).

2.3. Data storage

Each acquired pulse on any channel is tagged and stored with the channel number from where it was generated and the time at which the trigger occurred.

These modules provide a large storage capability of 1 GB for both raw data (array of sampled pulses) and processed data, which covers all the foreseen scenarios of acquisition time during a JET pulse. Continuous storage of 8 B at 200 MHz acquisition rate (1.6 GB/s) is provided through the interface to the DDR memory that is capable of a maximum of 3.2 GB/s.

3. Calibration

To achieve the desired resolution it is required to calibrate single channel errors and cross channel mismatching. The calibration consists in the calculation of a transfer function of each channel in order to correct the ADC output [6].

The algorithms for obtaining the transfer functions are under study using MATLAB® simulation and include frequency analysis and statistical amplitude measurements, for gain and offset corrections. The aim is to obtain an optimal algorithm to be implemented in the FPGA for on-line calibration.

4. Data processing

This system pretends to perform pulse analysis using complex algorithms applied to the digital equivalent of the collected pulses, implemented in the FPGA:

(i) pulse height analysis, the peak height of the pulse is of prime concern. Using several digital processing algorithms, like moving average, triangular or trapezoidal filter, a histogram of the pulse amplitudes can be done. Pile-up events are also detected and rejected; (ii) pulse shape discrimination, this technique will be based on the pulse area as a shape parameter using the charge integration method. Differences between the integrated charge in the entire pulse and integrated charge over the rising/falling portion are measured. Pulse height and total pulse area can be the same for both neutrons and γ rays, but the ratio between the total pulse and the rising/falling portion areas should be different depending on the reaction that took place [7].

5. Final considerations

This ND modular data acquisition system will be improved with two more TR modules based on the same interleaved architecture of the above described TR–TD: (i) two channels sampling at 200 MSPS at 14 b (higher bit resolution at the cost of lower sampling rate); (ii) two channels sampling at 2 GSPS at 8 b (higher sampling rate at the cost of lower bit resolution) including 0.5 ns resolution time digitizer.

State of the art modules like for instance the NI PCI-5911 high speed digitizer from Analog Devices [8] not only features pulse digitization but also the stamping of the same pulses permitting the random interleaved sampling, increasing the apparent sample rate of repetitive signals. The module presented here features an even more accurate pulse shaping and pulse temporal positioning.

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