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Ultra high-frequency data acquisition AMC module for high performance applications

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HIGHLIGHTS

- Advanced mezzanine card (AMC).
- FPGA mezzanine card (FMC).
- Ultra high-speed ADC: dual-channel sampling rate up to 1.6 GSPS at 10/12-bit or single-channel up to 3.2 GSPS at 10/12-bit.
- Support of multiple switch fabric protocols (PCIe, SRIO, and GigE).
- Module management controller.

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ABSTRACT

This paper describes the design and implementation of an ultra high-frequency data acquisition advanced mezzanine card (AMC) module, suitable for use in micro advanced telecommunications computing architecture (μATCA) and ATCA systems. This module is designed to meet the processing needs of high-performance applications required by the fast plant system controllers. It is also designed for high-availability (HA) and is envisaged to be used by the next generation of nuclear fusion diagnostics (e.g. as microwave reflectometry, plasma position reflectometry and Thomson scattering), foreseen for future fusion devices like the International Thermonuclear Experimental Reactor (ITER) tokamak or the Wendelstein 7-X (W7X) stellarator.

The developed module is a full size AMC designed to cope with the PICMG® AMC.0 R2.0 specifications. All the architecture is based on the ultra high-speed ADC that allows dual-channel sampling rate up to 1.0/1.6 GSPS at 10/12-bit or a single-channel up to 2.0/3.2 GSPS at 10/12-bit. The AMC module features a Field Programmable Gate Array (FPGA), Virtex™-6 from Xilinx that is able to manage high-speed data paths and implement high data rate processing algorithms. This FPGA supports multiple switch fabric protocols (PCIe, SRIO, and GigE). The module features also up to 2 GB of double data rate (DDR3) memory for data storage and 128 MB DDR3 memory for general purpose application, like, for instance, a soft processor core or digital filters. Also, a module management controller (MMC), required by the AMC standard, is implemented on-board to monitor the available and required hardware system management parameters.

1. Introduction

The next generation of nuclear fusion devices, like for instance tokamak ITER and the stellarator W7-X, are large-scale experiments with long duration plasmas discharges that will require systems with high levels of reliability and availability. ITER as well as W7-X are planned to operate with up to 30 min of continuous plasma discharges, being continuous operation the ultimate goal. Until today, the longest plasma discharge obtained with present fusion machines was observed at Joint European Torus (JET) tokamak, over almost a minute (~50 s) [1]. These complex experiments have similar requirements to apply to the several new diagnostic tools [2]. The just mentioned diagnostics tools are used to measure basic plasma quantities with both high temporal and spatial resolutions. All diagnostics will feature new Control and/or Data AcQuistion (CDAQ) systems designed to surpass the long/continuous operation

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time. CDAQ systems will provide: (i) redundant communications ports and synchronism signals allowing partial fails; (ii) intelligent management platform in charge of hot-swap maintenance, hardware/firmware configuration and board health monitoring; (iii) very large local storage capacity; (iv) high I/O channel count; (v) high-performance processing capabilities to prevent data loss; and (vi) low latency for real-time control.

Instituto de Plasmas e Fusão Nuclear (IPFN) [3] has undertaken a research programme, which envisages the specification phase and development of high-availability CDAQ systems for ITER. Therefore, IPFN is developing a prototype of a fast control plant system (FPSC) applicable to several diagnostic systems targeting plasma control. This FPSC is being implemented using ATCA based hardware. The ATCA based solution is challenging due to the lack of availability of Commercial-Off-The Shelf (COTS) solutions compliant with PICMG 3.4 specification (PCIe on fabric). PCIe on ATCA backplane fabric is a crucial feature for control systems as it will decrease data transport latency figures in contrast with the Ethernet data transfer solutions. Using Ethernet solely on the ATCA backplane for board-to-board interconnection would increase the software complexity and requires a processor in each board [4].

IPFN current development of hardware solution comprises: (i) an AMC carrier/PCIe switch and timing hub card (PICMG 3.0/3.4) [5]; (ii) a rear transition module (RTM) card with PCIe external cable interface; and (iii) an ATCA/PCIe node card (PICMG 3.0/3.4), with multi-channel hot-swappable digitizer (24–48 channels), designed for serviceability with connectivity on RTM [6].

Although the availability and diversity of COTS AMC products may be immediately integrated in the AMC carrier, one of IPFN' s goal is to achieve a complete in-house system. This goal is accomplished by adding to its product portfolio an ultra-high frequency data acquisition solution to cover such demanding diagnostics. One example is the Thomson Scattering (TS) diagnostic, installed at ASDEX and COMPASS based on 1 Giga Sample Per Second (GSPS) converters [7,8]. Another example, at slightly lower rate, is the frequency-modulated continuous-wave reflectometry diagnostic based on transient recorders of 250 MSPS, design for COMPASS [9], for applications foreseeing plasma. The two referred data acquisition solutions have in common, as key requirement, the need of a FPGA for high-rate data management and differ on its front-end. Therefore an AMC module with expansion connector is designed and developed.

This contribution describes the design and implementation of: (i) a full-size AMC module compliant to PICMG AMC.0 R2.0 [10] featuring a powerful FPGA, Virtex™ 6 from Xilinx, and adopting the ANSI/VITA57 standard for the extension connector, in order to accommodate a FPGA mezzanine card (FMC) [11], allowing an even more versatile architecture for the FPSC, and (ii) a single-width FMC module featuring a two 12-bit channel, ultra high-frequency analog to digital converter (ADC) that can achieve up to 1.6 GSPS or one 12-bit channel (interleave mode) up to 3.2 GSPS.

2. AMC carrier

The AMC module is designed to be inserted on the AMC carrier developed by IPFN (ATCA-PTSW-AMC4). Up to four AMC modules can be inserted. The carrier acts as a PCIe switch that allows the interconnection of: (i) 13 fabric channels (4× links), connecting up to other 13 PCIe (PICMG 3.4) compliant modules; (b) one 4× PCIe links to each AMC module; (c) one 4× PCIe link to the on-board FPGA; and (d) one 16× link to the RTM module (which is the interface to the system host). The ATCA-PTSW-AMC4 also performs timing signal distribution implemented on a Virtex™-6 FPGA, which manages and routes the ATCA, AMC and RTM timing clock lines [5]. The module ATCA-PTSW-AMC4 is shown in Fig. 1.

2.1. Clock and synchronization of the AMC modules

The PICMG defines mandatory timing and synchronization signalling between the carrier card and the AMC module, as so, the AMC clock interface is comprised of four quality level Telecom clocks (TCLKA, TCLKB, TCLKC and TCLKD) plus one fabric clock (FCLKA), this last one used for data transfer protocols. In fact the

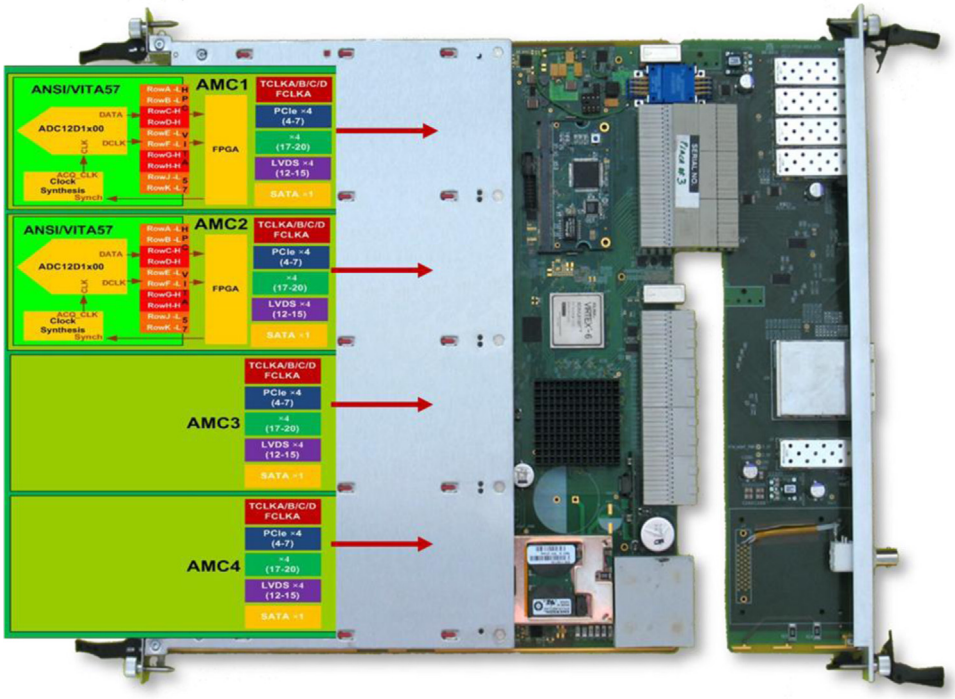

Fig. 1. Carrier AMC-IO module. Four AMC modules can be inserted.

carrier module acts as a clock distribution hub, as each clock line acts as a point-to-point connection. Either the carrier or the AMC module can be the clock receiver or transmitter, depending on the application. These clock links are dynamically configured, being issued by the corresponding carrier intellectual platform management controller (IPMC) and/or module management controller (MMC) [10].

The timing and synchronization signalling configuration for the described AMC carrier to AMC module is as follows: (i) the synchronization clock allows all the system channels to be synchronized; (ii) the trigger signal starts synchronously the acquisition of different AMC modules; (iii) absolute time information is sent by carrier coded in IRIG format (obtained from the Instrumentation Group time code) to all AMC modules; finally, and (iv) the data transfer protocol established between the carrier and the AMC module is PCIe, as so, the fabric clock is assigned to the PCIe clock, provided by the system root complex (for the described design the root complex is connected to the RTM).

3. Board implementation

The aim of this contribution is to describe an AMC module based on FPGA, which implements complex input/output (IO) interfaces and performs in-stream data processing (AMC-IO). In order to reduce costs and development time, FMC standard appears as a small add-on module to provide different front-ends for AMC modules with FPGAs. This FMC module is an ultra-high speed analog-to-digital (AD) converter front-end (FMC-AD), but other FMCs can be added, like for instance, lower rate AD converter modules, digital-to-analog modules, processor modules, connectivity modules which break out the FPGA multi-gigabit transceiver (MGT) interface signals to and from the module interface, and other type of modules.

3.1. AMC-IO module

This module is a full-size AMC, featuring: (i) one Virtex™-6 FPGA, for data management and high-performance processing applications; (ii) one standard DDR3 Synchronous Dynamic Random Access Memory (SDRAM) SODIMM memory up to 2 GB; (iii) one DDR3 SDRAM component of 128 MB for future MicroBlaze™ applications (FPGA-based soft processor); (iv) one Platform flash XL, a 128 MB (8 MB 16×) non-volatile flash memory for FPGA configuration and MicroBlaze™ boot code; (v) a high-pin count (HPC) extension connector, enabling a broad range of I/O interfaces to be added to meet several application needs, adopting the FMC ANSI/VITA57 standard; (vi) power supply distribution according to the maximum power rate (the standard limits AMC modules to 60 W of power consumption); (vii) clock generation and distribution; (viii) temperature sensors; and finally (ix) the MMC implemented on-board by using a microcontroller based on a 32-bit ARM7 CPU from NPX. The microcontroller monitors the required and available hardware system management parameters, for instance, the FPGA and board temperatures, the ADC temperature, board hot-swap and others. The AMC module diagram block is shown in Fig. 2.

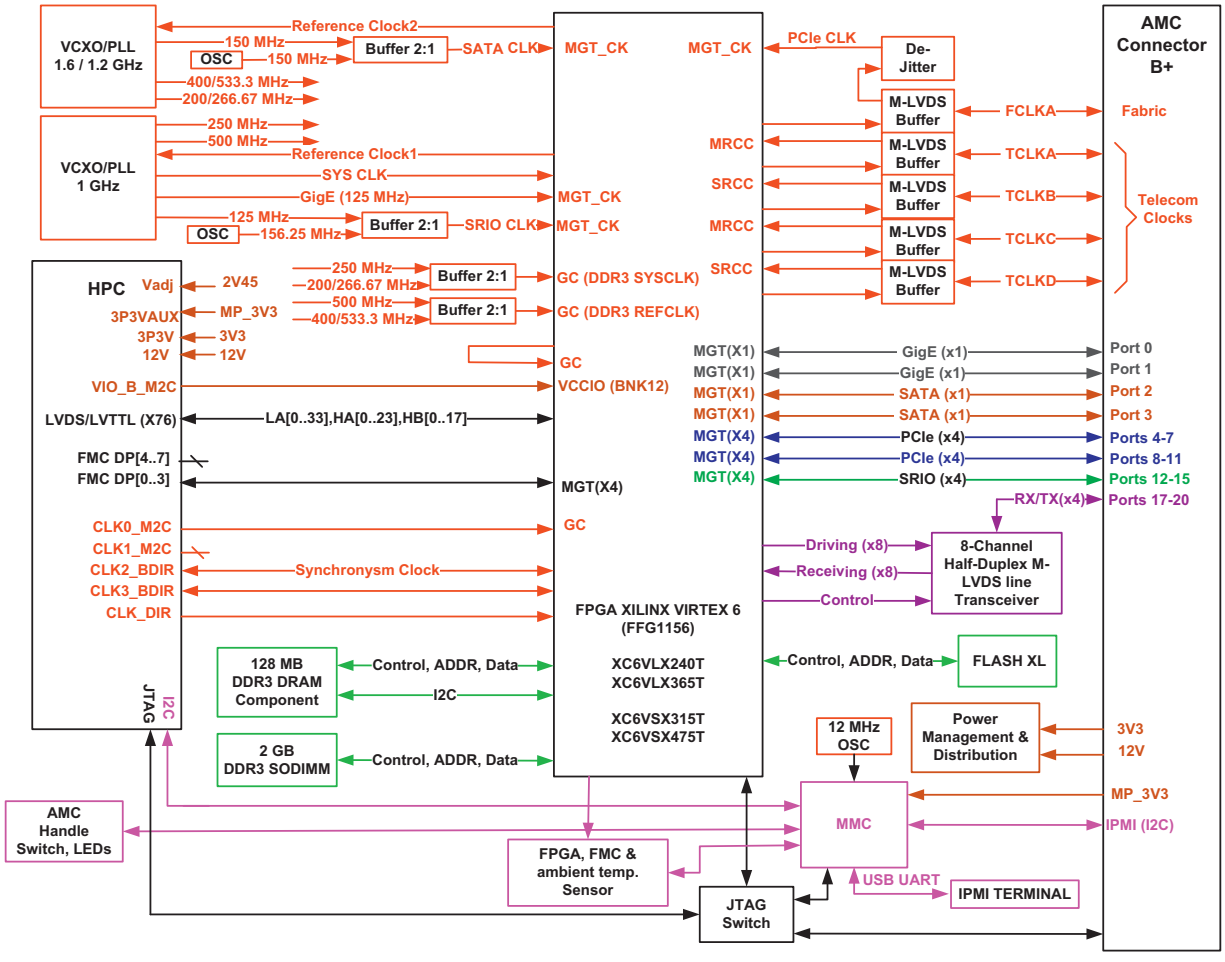

Fig. 2. Diagram block of the AMC-IO module.

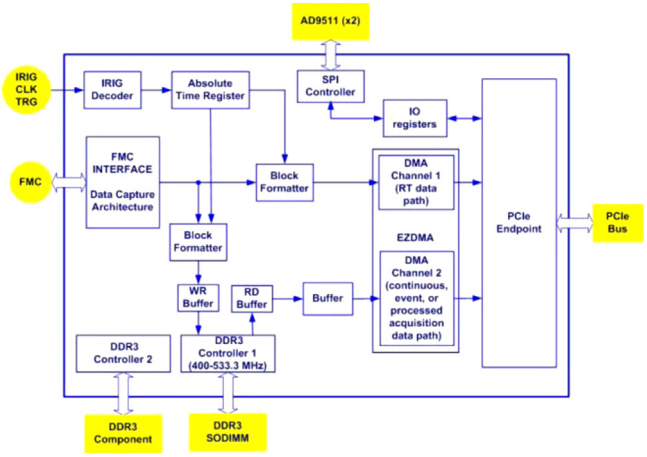

Fig. 3. FPGA architecture of the AMC-IO module.

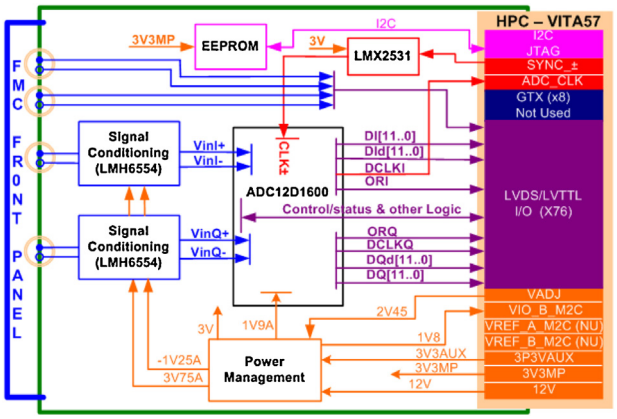

Fig. 4. FMC-AD1600 module diagram block.

The ANSI/VITA57 standard defines four differential reference clocks: two differential clocks provided by the FMC Module to the AMC Carrier (M2C), CLK0_M2C and CLK1_M2C, and two differential clocks dependent of the CLK_DIR signal, CLK2_BDIR, and CLK3_BDIR. If CLK_DIR is connected to ground on the FMC (or left unconnected), then all clock pairs are M2C provided. Else the clocks are provided by the AMC carrier to the FMC module (C2M), like, for instance, the system synchronization clock. Due to the AMC module firmware architecture, that allows the DDR3 to operate at a maximum rate of 533.33 MHz, only one global clock is available at the FPGA to be assigned to the expansion connector, CLK3_C2M. To conclude, the AMC module supports only one receiving clock and provides two transmitting clocks.

Concerning the gigabit interfaces, AMC connectivity architecture is defined as follows: (i) 4× PCIe at ports 4–7 at the AMC connector B+ and the possibility to extend the PCIe link to 8× (ports 8–11); (ii) 4× SRIO links at ports 12–15; (iii) two storage 1× links at ports 2 and 3; and (iv) two gigabit ethernet 1× links at ports 0 and 1. All these ports are connected to the FPGA MGTs. This AMC module provides only 4 of the 8× gigabit links specified by ANSI/VITA57 standard to the expansion connector. These connections are shown in Fig. 2.

3.1.1. Firmware

The FPGA firmware is based on digitizer architecture, being the digitized inputs provided by the FMC. Though the firmware has: (i) a modular FMC interface, dependent on the FMC inserted on the expansion connector; (ii) 2 DMA channels, one for the real-time data transfer and the other for retrieving the data from the on-board memory; (iii) endpoint PCIe core; and (iv) two DDR3 memory controllers, allowing frequency range up to 533.3 MHz. A block diagram of the firmware architecture is depicted in Fig. 3.

All block samples are time stamped with the occurrence time correlated with the absolute time information. An internal time counter on each FPGA will be synchronized by the Synch clock (100 MHz) and IRIG signals transmitted by the carrier. For high-speed front-ends, the FPGA data capture architecture will be based on DDR data latching in order to de-mux and reduce data capture and path to frequencies within the capability of current FPGA technology.

3.2. FMC-AD module

This is a single-width, full-height FMC module featuring a configurable ADC from National Semiconductors, ADC1xD1x00 [12] (FMC-AD1x00), that can operate in an interleaved mode, one 10/12-bit channel at 2/3.2 GSPS, or normal mode, two 10/12-bit channels at 1/1.6 GSPS. This ADC provides a flexible low-voltage differential signalling (LVDS) interface, with programmable options to facilitate board design and FPGA data capture. For ease of integration, this ADC provides test patterns at output for debugging purposes. Also, interleaving ADC channels is a challenge for the hardware designer that has to be very careful with gain, phase and offset matching between each individual ADC channel, to keep its performance level. To cope with these 3 impact factors on the dynamic performance, this particular ADC features: (i) automatic timing consisting of clock phasing (180° intervals) and manual skew, to minimize clock jitter effects; (ii) a programmable 15-bit gain; and (iii) 12-bit plus sign offset. Furthermore, the FMC module has a special internal sampling clock generation design that also contributes to minimize clock jitter effects even at the highest sampling rates and resolution.

Another important limiting factor, in the overall system performance, is the choice of the amplifier which drives the ADC. Attention must be paid how to maximize the dynamic range and, at the same time, choose the best passive filter, at the ADC's input, for a specific application. Signal conditioning is implemented with a linear, fully differential amplifier to guarantee exceptional signal fidelity as well as large bandwidth. This design also allows single-ended to differential conversion to cope with single-ended systems.

The FMC-AD1x00 power rating is limited to 10 W by the standard. An electrical erasable programmable read-only memory (EEPROM) is also included, to store information pertaining to the characteristics of the FMC module relevant to the MMC. The block diagram of this module is presented in Fig. 4.

In the near future other front-end FMCs with different acquisition rates and number of channels are also foreseen.

4. Conclusions

The modularity of the described AMC module allows several solutions to be introduced in a short period of time, where only the FMC module and corresponding FMC interface firmware will need to be adapted to the new application. At a first glance, developing two modules instead of one appears to be more expensive, but in the near future the modularity will allow a wide number of solutions in a short implementing time.

Besides the modularity of the system, the major concern of this architecture is the capacity of processing such high-rate data as near as possible to the process. The powerful FPGA will apply for data reduction algorithms as well as supporting high-speed data transfer protocols to the system host. This will allow system operation, without data loss, during the 30 min plasma discharges foreseen for ITER.

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