
UNIVERSIDADE D
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# MODEL PREDICTIVE CONTROL OF PARALLEL CONNECTED UNINTERRUPTIBLE POWER SUPPLIES

Dissertation in the scope of the Integrated Master's in Electrical and Computer Engineering, branch of specialization of Energy supervised by Professor Doutor André Manuel dos Santos Mendes and co-supervised by Doutor Luís Miguel Antunes Caseiro and presented to the Faculty of Science and Technology / Department of Electrical and Computer Engineering.

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Dissertation submitted to the Electrical and Computer Engineering Department of the Faculty of Science and Technology of the University of Coimbra in partial fulfillment of the requirements for the Degree of Master of Science in Electrical and Computer Engineering.

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"However difficult life may seem, there is always something you can do, and succeed at. It matters that you don't just give up."

**Stephen Hawking**

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# Abstract

Nowadays, uninterruptible power supplies (UPS) play a key role in feeding the critical loads of electric power systems. Due to the continuous proliferation of such loads and higher sensitivity regarding undesired grid phenomena at the grid delivery point, UPS systems are frequently connected in parallel. Thus, high-power loads can be supplied with higher reliability and efficiency.

The main objective of a UPS is to permanently provide a high-quality voltage waveform to the load. This is also true when these systems are connected in parallel. However, when UPS systems are parallel-connected, two fundamental requirements must be verified to ensure a correct system operation: potential circulating currents between the two systems must be eliminated, and the load power must be distributed between the two systems accordingly to their availability.

This dissertation has as main objective the development of an algorithm to control two double conversion UPSs, connected in parallel. Both UPS systems present multilevel topology, with two 3-level Neutral Point Clamped converters (3LNPC).

Given its advantages, to control all the power converters, Finite Control Set Model Predictive Control (FCS-MPC) was selected.

The developed control strategy was tested in simulation and experimental environment. The obtained simulation and experimental results demonstrated the effectiveness of the proposed method. Each UPS system can provide a different percentage of the load power, eliminating the circulating current between the two paralleled systems and ensuring a high-quality load voltage waveform for linear and non-linear loads. For all the tested conditions, both UPSs show stable operation and fast dynamic response to variations regarding the load power distribution.

**Keywords:** predictive control, uninterruptible power supplies, multilevel converters, power quality.

# Resumo

Atualmente, as fontes de tensão ininterruptas (UPS) desempenham um papel fundamental na alimentação de diversas cargas críticas existentes nos sistemas de energia elétrica. Face ao continuo aumento destas cargas bem como da sua sensibilidade perante fenómenos indesejados que inevitavelmentel ocorrem nos pontos de entrega da rede elétrica, os sistemas UPS são recorrentemente ligados em paralelo. Desta forma, cargas de maior potência podem ser alimentadas com superior grau de fiabilidade e eficiência.

O principal objetivo de um sistema UPS é garantir, permanentemente, uma forma de onda de tensão de elevada qualidade na carga. O mesmo se verifica quando estes sistemas são ligados em paralelo. No entanto, quando duas UPS são ligadas em paralelo, existem dois requisitos fundamentais para o correto funcionamento do sistema nomeadamente a eliminação de potenciais correntes circulantes e uma distribuição controlada da potência absorvida pela carga pelas duas UPSs, de acordo com a sua disponibilidade.

Esta dissertação tem como principal objetivo o desenvolvimento de um algoritmo para controlar duas fontes de tensão ininterruptas (UPS) de dupla conversão, ligadas em paralelo. Ambas as UPS apresentam topologia multinível, sendo consituidas por dois conversores NPC de 3 níveis (3LNPC).

Face às suas vantagens, para controlar todos os conversores dos sistemas UPS foi utilizado controlo preditivo baseado em modelos de estados finitos (FCS-MPC).

A estratégia de controlo desenvolvida foi testada em ambiente de simulação e experimental. Os resultados de simulação bem como os resultados experimentais comprovam a eficácia do método proposto. Cada sistema UPS pode fornecer uma percentagem da potência total à carga, eliminando simultaneamente a corrente de circulação entre os dois sistemas e assegurando ainda uma forma de onda de tensão na carga de elevada qualidade, quer para cargas lineares como para cargas não lineares. Para as condições testadas, as UPS apresentam funcionamento estável e rápida resposta dinâmica a variações na distribuição da potência absorvida pela carga.

**Keywords:** controlo preditivo, fontes de tensão ininterruptas, conversores multinível, qualidade de serviço.

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# Symbols and Abbreviations

**Acronyms**

| | |
|---|---|
| 3LNPC | 3-level Neutral-Point-Clamped |
| BTB | Back-to-Back |
| CMV | Common Mode Voltage |
| FCS-MPC | Finite Control Set Model Predictive Control |
| IGBT | Insulated-Gate Bipolar Transistor |
| MPC | Model Predictive Control |
| NPC | Neutral-Point-Clamped |
| PF | Power Factor |
| PLL | Phase-Locked Loop |
| PWM | Pulse Width Modulation |
| THD | Total Harmonic Distortion |
| UPS | Uninterruptible Power Supply |
| ZSCC | Zero Sequence Circulating Current |

**Nomenclature**

| | |
|---|---|
| $X$ | Arbitrary phases of NPC converters $X \in \{R, S, T\}$ in the grid-side converters or $X \in \{A, B, C\}$ in the load-side converters |
| $x$ | Arbitrary variable $x$ |
| $x^*$ | Reference value of the arbitrary variable $x$ |
| $x^p$ | Predicted value of the arbitrary variable $x$ |
| $x_\alpha, x_\beta$ | Arbitrary three-phase variables in the stationary reference frame $\alpha\beta$ |

## Symbols

| | |
|---|---|
| $\lambda_1$ | Quote of the load power assigned to the UPS1 |
| $\lambda_2$ | Quote of the load power assigned to the UPS2 |
| $\overline{i}_g$ | Grid-side converter current space vector |
| $\overline{i}_L$ | Load-side converter current vector |
| $\overline{i}_{C_L}$ | Space vector of current in the load-side filter capacitors |
| $\overline{i}_{load}$ | Load current vector |
| $\overline{v}_g$ | Grid-side converter voltage space vector |
| $\overline{v}_L$ | Load-side converter voltage space vector |
| $\overline{v}_{load}$ | Load voltage vector |
| $C_1, C_2$ | DC bus capacitors |
| $C_L$ | Load-side filter capacitance |
| $C_{DC}$ | Capacitance value of DC bus capacitors |
| $G$ | Global objective function |
| $g_i$ | Objective function regarding the current |
| $g_{bal}$ | Objective function regarding the DC bus capacitor unbalance |
| $g_z$ | Objective function regarding the ZSCC |
| $i^p_{g_\alpha}, i^p_{g_\beta}$ | Predicted grid currents in the stationary reference frame $\alpha\beta$ |
| $i^p_{L_\alpha}, i^p_{L_\beta}$ | Predicted load-side converter currents in the stationary reference frame |
| $i_0$ | Zero Sequence Circulating Current |
| $i_A, i_B, i_C$ | Load-side converter currents |
| $i_R, i_S, i_T$ | Grid-side converter currents |
| $i_X$ | Line current in phase X Line current in phase $X$ |
| $i_{C_1}, i_{C_2}$ | DC bus capacitor currents |
| $i_{g_\alpha}, i_{g_\beta}$ | Grid currents in the stationary reference frame |

| | |
|---|---|
| $i_{L_\alpha}, i_{L_\beta}$ | Load-side converter currents in the stationary reference frame |
| $i_{P_G}, i_{M_G}, i_{N_G}$ | Currents supplied to the DC bus by the grid-side converter |
| $i_{P_L}, i_{M_L}, i_{N_L}$ | Currents drawn from the DC bus by the load-side converter |
| $L_G, R_G$ | Grid-side filter parameters (inductance and resistance) |
| $L_L, R_L$ | Load-side filter inductor parameters (inductance and resistance) |
| $N_{charge}$ | Horizon for DC bus charging (number of samples) |
| $P_g$ | Active power supplied by the grid-side converter to the DC bus |
| $P_{charge}$ | Active power component responsible for charging the DC bus |
| $P_{grid}$ | Active power drawn by the load-side converter from the DC bus |
| $P_{load}$ | Active power supplied to the load |
| $P_L$ | Active power component responsible for charging the DC bus |
| $S_X$ | Switching state in phase X |
| $v^p_{C_1}, v^p_{C_2}$ | DC bus capacitor voltages |
| $v^p_{C_1}, v^p_{C_2}$ | Predicted DC bus capacitor voltages |
| $v^p_{load_\alpha}, v^p_{load_\beta}$ | Predicted load voltages in the stationary reference frame $\alpha\beta$ |
| $v^p_{s_\alpha}, v^p_{s_\beta}$ | Predicted supply voltages in the stationary reference frame $\alpha\beta$ |
| $v_s$ | Supply voltage space vector |
| $v_{AM}, v_{BM}, v_{CM}$ | Pole voltages of the load-side converters |
| $v_{C_1}, v_{C_2}$ | DC bus capacitor voltages |
| $v_{DC}$ | DC bus voltage |
| $v_{g_\alpha}, v_{g_\beta}$ | Grid-side converter voltages in the stationary reference frame $\alpha\beta$ |
| $v_{L_\alpha}, v_{L_\beta}$ | Load-side converter voltages in the stationary reference frame $\alpha\beta$ |
| $v_{load_\alpha}, v_{load_\beta}$ | Load voltages in the stationary reference frame $\alpha\beta$ |
| $v_{load_A}, v_{load_B}, v_{load_C}$ | Load phase voltages |
| $v_{load_{AB}}, v_{load_{BC}}, v_{load_{CA}}$ | Load line-to-line voltages |
| $v_{OM}$ | Converter common mode voltage |

| | |
|---|---|
| $v_{RM}, v_{SM}, v_{TM}$ | Load line-to-line voltages |
| $v_{s_\alpha}, v_{s_\beta}$ | Supply voltages in the stationary reference frame $\alpha\beta$ |
| $v_{s_R}, v_{s_S}, v_{s_T}$ | Supply phase voltages |
| $v_{s_{RS}}, v_{s_{ST}}, v_{s_{TR}}$ | Supply line-to-line voltages |
| $v_{XM}$ | Pole voltage in phase $X$ |
| $W_i$ | Weighting factor regarding current |
| $W_{bal}$ | Weighting factor regarding DC bus capacitors balance |
| $W_z$ | Weighting factor regarding ZSCC |

# Chapter 1

# Introduction

## 1.1 Motivation and Context

During the last years, the proliferation of new and ever more important electrical loads has created an energetic demand for highly reliable power sources. Despite the high reliability provided by electrical grids nowadays (mostly in the developed countries), undesirable grid events from voltage oscillations to supply interruptions, cannot be completely avoided.

In a power system, the unplanned interruption of critical loads can lead to very undesirable consequences. Information and communication centers, hospitals and industrial electrical equipment are examples of critical loads. These loads must be continuously supplied. In the light of these facts, uninterruptible power supplies (UPS) are seen as a great solution to protect critical loads from supply interruptions. In some cases the quality of the delivered power must respect strict requirements. Therefore, additional protection to the load regarding undesired grid phenomena can also be provided by some types of UPS.

The use of multilevel converts in UPS systems is being adopted as a way to increase the overall system performance. A UPS based on multilevel converters absorbs current and generates voltage with lower harmonic distortion compared to a two-level based UPS. By using multilevel converters, the cost of a UPS can even be decreased since cheaper and smaller filters are typically needed.

Nowadays, UPS systems are employed to a wide range of electrical loads: from low-power applications (as domestic computers and networks) to high-power applications of several Megawatt (as IT centers and medical facilities).

The use of paralleled UPS is getting more and more popular as a way to improve system power rating, efficiency and reliability. However, in general, when power electronic converters are paralleled, two big concerns arise: potential undesirable circulating currents must be suppressed and the total current absorbed by the load must be distributed between the paralleled systems according to their availability.

The possibility of having an asymmetric load power distribution is very important due to efficiency and reliability reasons. The efficiency of a power conversion system increases

with the load. When a power electronics converter operates at low load, power losses become more significant, leading to low efficiency values. Therefore, in paralleled converters, an asymmetric power distribution can increase the overall system efficiency. Moreover, if one converter is not able to supply its power target (for example due to a fault), then the other converters must increase their target power, to maintain the system correct operation.

The main objective of this dissertation is to develop a control strategy for two paralleled *double conversion* UPSs which are based on multilevel converters.

## 1.2 Main Contributions

A lot of studies can be found in the literature regarding the parallel of UPSs based on two-level converters. However, severe limitations regarding asymmetric load-sharing control strategies and circulating current suppression in UPSs based on multilevel converters still exist. The majority of such studies have as main concern the distribution of the load current equally between the paralleled systems to naturally avoid potential circulating currents. Moreover, the dynamics of the circulating currents in UPSs based on multilevel converters, as well as strategies for its suppression are still not defined.

The main controller priority of a UPS system is to generate a high-quality output voltage waveform. Therefore, output voltage is usually directly controlled in finite control-set model predictive control (FCS-MPC) [1–3]. However, when two UPSs are paralleled, controlling the output voltage directly does not allow a direct load-sharing control.

In this dissertation a paralleled system based on two *double conversion* UPSs is proposed. Using FCS-MPC, the developed strategy allows asymmetric distribution of the load power between the two paralleled UPSs and simultaneous circulating current suppression. In the proposed control strategy, the output currents are directly controlled, ensuring a controlled power distribution between UPSs and simultaneously a high quality load voltage waveform.

## 1.3 Goals

In this work, the parallel operation of two UPSs based on multilevel converters is studied. Hence, the defined goals for this dissertation are:

- to develop a FCS-MPC based algorithm to control the paralleled UPSs. The algorithm must simultaneously ensure: a high-quality load voltage waveform, the possibility of an asymmetric load-sharing and circulating current suppression;
- to realize simulation tests that evaluate the effectiveness of the developed algorithm;
- to rearrange and combine two experimental prototypes;
- to implement the developed algorithm in a real controller.

## 1.4 Structure

This dissertation contains five chapters. In Chapter 1 the motivation, main contributions and goals of this work are presented.

Chapter 2 is dedicated to a literature review of the main topics regarding this work. A brief description of the available power converters control strategies is made, with additional emphasis to the operation principle of FCS-MPC. The types of UPS and their main differences are also presented. Then, the main control schemes used for parallel-connected UPSs are discussed. Finally, the adopted system configuration is presented.

In Chapter 3 the mathematical model of the paralleled system and the dynamics of the circulating current are presented. The discretized model equations and the principles of FCS-MPC are also demonstrated.

In Chapter 4 the simulation and experimental results are presented and discussed. The performance of each UPS is firstly demonstrated. Then, the effectiveness of the developed algorithm is presented in terms of circulating current suppression and load-sharing precision.

Finally, Chapter 5 presents the conclusions of the dissertation as well as potential topics for future work.

# Chapter 2

# State of the art

## 2.1 Power converters control strategies

Over the last decades, intense research and significant advances made on digital controllers, have allowed the development of high performance techniques that require high computational power processing [4]. The most common types of control strategies used for power electronics converters are depicted in Figure 2.1.

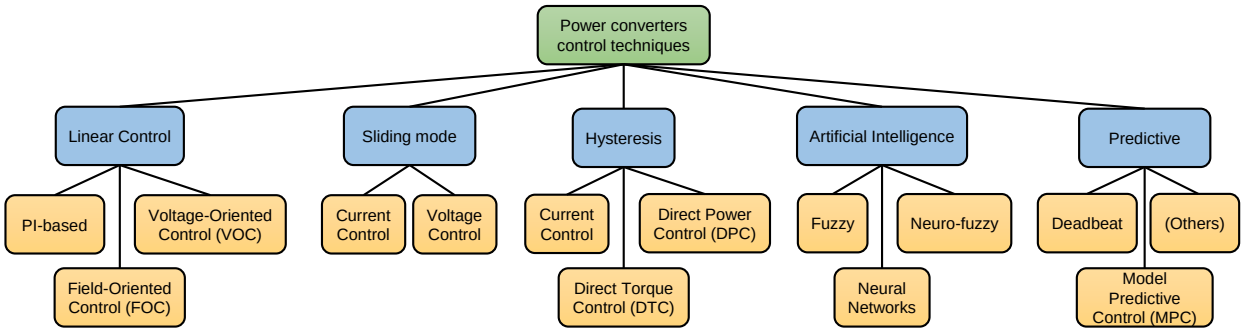



Figure 2.1: Classification of control techniques used for power electronics converters (adapted from [5]).

Linear control strategies are widely used in power electronics. The most common linear control scheme is the adoption of a proportional-integral controller (PI) and a modulator. However, for electric drives and grid-connected applications, the field-oriented control (FOC) [6] and voltage-oriented control (VOC) [7] are also used. A significant drawback of the linear controllers is the fact that the inclusion of system non-linearities and constraints can lead to very complex control schemes. Thus, for some systems, this control technique may provide poor transient response and protection.

In a hysteresis based control scheme, an error band is defined around a reference value. In each control cycle, the controller verifies if the respective control variable is within the hysteresis band and applies the switching state to the converter accordingly. The direct power control (DPC) [8] and direct torque control (DTC) [9] techniques are solutions that

use this kind of non-linear concept, however simpler strategies based on hysteresis current control can also be found [10].

The linear and hysteresis control techniques are nowadays truly integrated in the academic community and greatly adopted in the industry.

The remaining three types of control techniques are now mainly under research and have been gradually adopted along with the ever increasing power processing of the microprocessors. From those three types of control, predictive control has taken some advantage over sliding mode control and artificial-intelligence based methods. The use of sliding mode control in power electronic converters is still very scarce mainly due to high-frequency oscillation problems [11]. In the artificial intelligence based methods, system non-linearities can be easily integrated. However, a pre-training stage is required to generate the machine learning classifier, which might provide low control flexibility [12].

The predictive control concept is very simple and intuitive [13]: from the mathematical model of the system, the future value of the control variables are predicted. The prediction is made considering all the power converter switching states. The switching state that optimizes a set of predefined control objectives is chosen by the controller and applied to the converter. Using predictive control very fast transient responses are achieved and the system non-linearities and constraints are easily included in the control scheme.

Predictive control methods are typically classified into four sub-groups: deadbeat, trajectory- and hysteresis-based predictive control, and finally model predictive control (MPC). The deadbeat control requires a modulator. In this type of control, the inverter voltage that would eliminate the error of a certain control variable regarding the respective reference in only one control sample time is calculated and sent to a modulator that generates the intended voltage [14]. Both the hysteresis and the trajectory predictive control requires no modulator. In hysteresis-based predictive control the switching states are selected so that a set of variables are maintained within a predefined hysteresis band [15]. In the trajectory-based predictive control, the switching states are selected so that the control variables follow a given trajectory [16]. Finally, the model predictive control technique consists in the minimization of a objective function (also known as cost function) over a given prediction horizon [13]. Inside MPC, two types of control are defined depending on the considered control set, that can be continuous (CCS-MPC) or finite (FCS-MPC). If a continuous control set is adopted, the continuous action of the controller is considered and a modulator is required. Otherwise, if a finite control set is adopted, no modulator is required and only the finite amount of the converter switching states is taken into consideration by the controller (considerably simplifying algorithm design). Compared to CCS-MPC, FCS-MPC allows an easier implementation of the system non-linearities and integration of control constraints. In light of these facts, FCS-MPC is adopted in this dissertation to control all power converters of the paralleled UPSs.

### 2.1.1 Finite Control Set Model Predictive Control

FCS-MPC uses the mathematical model of the system to predict the future value of the controlled variables considering all the possible converter switching states. The switching state that optimizes the system operation is therefore applied to the converter. Figure 2.2 depicts the FCS-MPC principle considering a prediction horizon of one sample. As illustrated, at sample $k$ the value of variable $x$ at sample $k+1$ is estimated for all possible converter switching states. An objective function is defined as

$$g = |x^*[k+1] - x^p[k+1]|\,,$$

where $x^*[k+1]$ and $x^p[k+1]$ are respectively the reference and the predicted value of the variable $x$ at $k+1$. The control state that minimizes the objective function is selected for application in the converter. This process is repeated at $k+1$ to optimized the system state at sample $k+2$, and so on. Hence, by choosing the switching state that optimizes the system operation at every sampling time, FCS-MPC provides fast transient response and high steady-state performance.

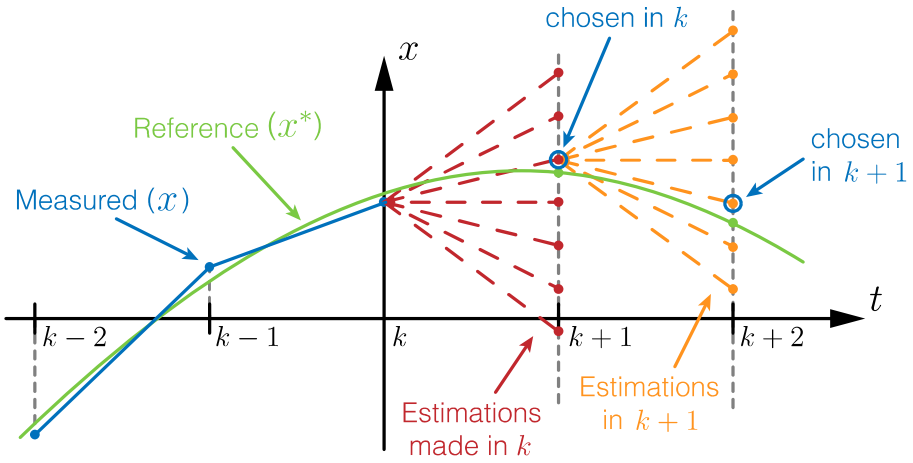



Figure 2.2: FCS-MPC operation principle illustration (adapted from [2]).

Several cost functions can be considered depending on the system complexity. Therefore, a global objective function can be defined as a linear combination of several weighted partial cost functions,

$$g = W_1 g_1 + W_2 g_2 + ... + W_n g_n\,,$$

where $W_1, W_2, ..., W_n$ are the predefined weighting factors of partial cost functions $g_1, g_2, ..., g_n$. These coefficients are of great importance since they define the importance of each control variable and provide magnitude correction between them.

FCS-MPC provides great capability of response to adverse situations, due to an easy introduction of constraints in the control scheme. For instance, the penalization introduced by a partial function in the global cost function can be increased when a variable exceeds

a predefined limit. This gives full priority to the respective partial objective function, and represents a way of ensuring additional protection to the converter that is being controlled.

Compared to classic linear controllers such as the PI-based ones, which are tuned for a specific operation point, the FCS-MPC provide faster transient response in a wider operation range. The adoption of this control scheme is also interesting for systems with more than one power converter: the control action of one converter can be taken into account on the objective function of the second converter [2, 1]. This cooperation principle usually increases the overall system performance and stability. For all these reasons, FCS-MPC has been greatly accepted and further developed by scientific community being nowadays considered as a control solution capable of providing equivalent or higher performance over other control techniques such as conventional linear voltage control [17–19] and hysteresis based control [20].

Even so, some limiting factors can still be found to the implementation of FCS-MPC. Given the amount of calculations involved, to provide very high performance this type of control usually requires controllers with high power processing capabilities, especially in complex systems, such as those with multilevel converters or multiple converters. Another disadvantage is the fact that for a proper control operation the system parameters must be accurately known and the mathematical model totally defined, which for some systems can be very difficult to achieve. Finally, one of the most challenging topics that can severally affect both the dynamic and steady-state performance of the control is the correct choice of the weighting factors [21].

## 2.2 Multilevel converters

Multilevel converters have a lot of advantages when compared to the conventional 2-level converters [22]. As the number of levels in output voltage increases, lower voltage and current distortion is produced. To provide the same performance than a multilevel converter, a two-level converter usually presents higher switching losses due to the required higher amount of commutations. Given the fact that the DC bus voltage is distributed through a high number of semiconductors, higher voltage ratings are also achieved in systems that use multilevel converters. Figure 2.3 shows the circuit representation of a three-level neutral point clamped (3LNPC) converter. From all available three-level converter configurations, this is the most used in industry [23]. Hence, all the power converters used in this work have the represented configuration. The 3LNPC can generate three different voltage levels between a phase terminal and the middle point of the DC bus. As a multilevel converter, the 3LNPC have been object of intense research [23] in the last few decades as well as their use in back-to-back (BTB) topologies [24–26].

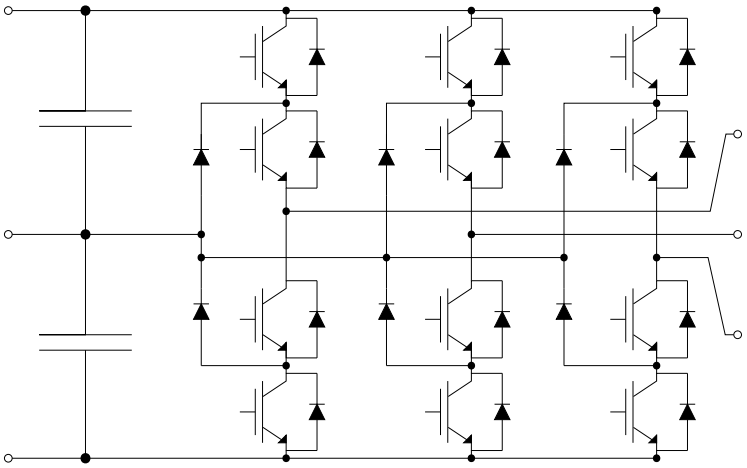


Figure 2.3: Representation of a three-level neutral point clamped (3LNPC) power converter.

## 2.3 Uninterruptible Power Supplies

### 2.3.1 Types of UPS

The main types of UPS are shown in Figure 2.4. Typically, a UPS can be classified as a rotary or static UPS. However, given the low flexibility of a rotary UPS, hybrid configurations can also be found as Figure 2.5 illustrates.

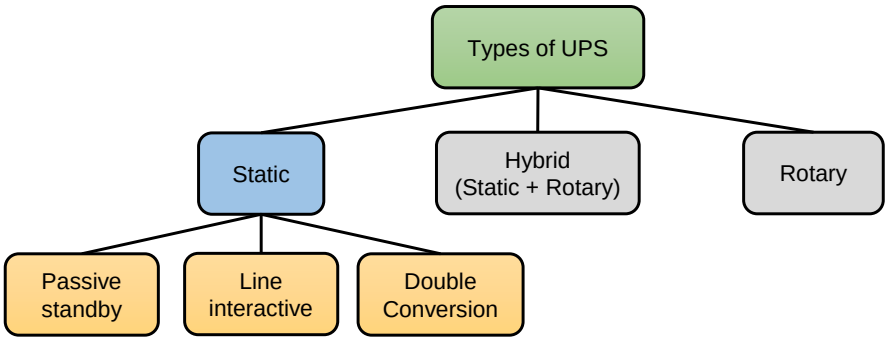
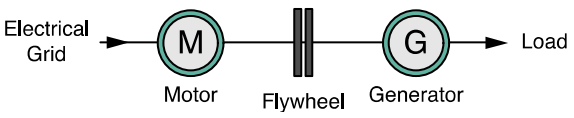
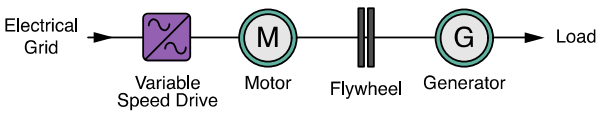



Figure 2.4: Types of uninterruptible power supplies.

Rotary and hybrid UPS have been used over the last years mainly by virtue of their very high power ratings. However, these system are nowadays rarely used mainly because of their high maintenance costs and low efficiency (high mechanical losses).




(a) Rotary UPS illustration.



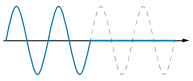
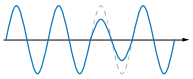
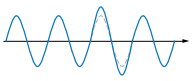
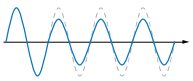
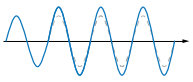
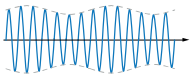
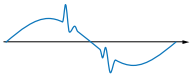
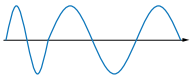
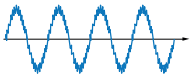
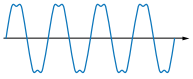
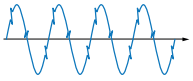

(b) Hybrid UPS illustration.

Figure 2.5: Typical layout of rotary and hybrid UPS (adapted from [2]).

Through out the years, the evolution of semiconductor components and consequently of power electronics converts lead to the development of static UPSs. When compared to the

rotary systems, static UPS provide higher reliability and efficiency, better transient response, lower maintenance costs and reduced noise level [27]. According to the European Guide for Uninterruptible Power Supplies [28], 95 % of the UPS sold are static being 98 % of them used for IT and other electrical applications. As Table 2.1 shows, the international standard IEC 62040-3, divides the static UPS into three categories [29]: *passive standby*, *line-interactive* and *double conversion*. This classification mainly depends on the degree of protection that the system can provide to the load as well as how much the system is independent from the grid voltage and frequency.

Table 2.1: Power quality problems and IEC 62040-3 UPS classification [2].

| **Power line problems** | **Waveform** | **UPS type** | | **IEC 62040-3 classification** | | | |
|---|---|---|---|---|---|---|---|
| Line failure (supply interruption : > 10 ms) |  | **Passive Standby** | Voltage and Frequency Dependent (VFD) | **Line Interactive** | Voltage Independent (VI) | **Double Conversion** | Voltage and Frequency Independent (VFI) |
| Sag or Dip (short under-voltage : < 16 ms) |  | | | | | | |
| Surge (short over-voltage : < 16 ms) |  | | | | | | |
| Under-voltage (for long periods) |  | | | | | | |
| Over-voltage (for long periods) |  | | | | | | |
| Flicker |  | | | | | | |
| Transient, impulse or spike (up to a few ns) |  | | | | | | |
| Frequency variation |  | | | | | | |
| Noise |  | | | | | | |
| Harmonic distortion |  | | | | | | |
| Notching (caused by switching or fast current change) |  | | | | | | |

The typical configuration of a *passive standby* UPS is represented in Figure 2.6. This type of UPS provides the lowest level of protection to the load. During the normal operation, the grid directly feeds the load and charges the UPS batteries. When the grid voltage waveform doesn't respect predefined thresholds, the load is transferred to the output of the UPS.

After the commutation, the load is fed with the energy previously stored in the batteries. Since the commutation time is above 10 ms, and during the normal operation the system cannot change the load voltage amplitude and frequency, this type of UPS is not employed in sensitive high-power critical loads. Instead, a *passive standby* UPS is mainly used in low power applications (below 1kVA) such as personal computers and private networks [2].

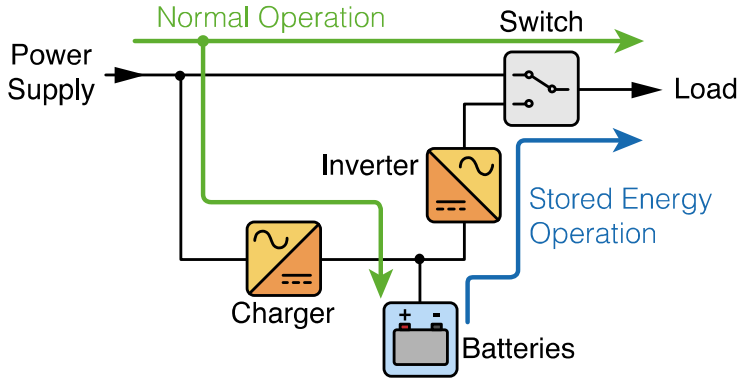



Figure 2.6: Typical configuration of a passive standby UPS [2].

In Figure 2.7 the typical configuration of a *line interactive* UPS is shown. This type of UPS works identically to the *passive standby* UPS: when the grid goes out from predefined limits, the load power is entirely provided by the batteries. However, in this type of systems, a bidirectional converter is usually used . Using this converter, the load can be supplied by the batteries and by the grid simultaneously during the normal operation mode. Hence, the bidirectional converter provides load voltage correction capabilities. However, frequency related problems cannot be avoided and therefore the load still stays vulnerable to a set of grid problems like voltage noise and harmonic distortion. Even so, this type of UPS is usually adopted in medium power IT applications and other small businesses (below 20 kVA) [2].

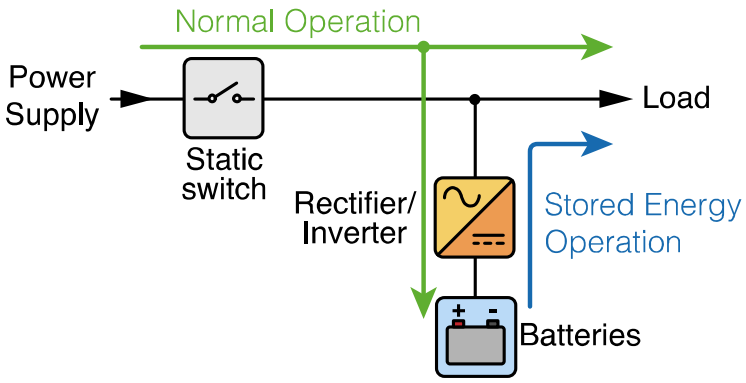



Figure 2.7: Typical configuration of a line-interactive UPS [2].

Finally, the *double conversion* UPS configuration is represented in Figure 2.8. This is the most reliable type of UPS, since all the power supplied to the load flows through the power converters. With this configuration the load voltage waveform is totally independent

from the grid voltage waveform. Thus, the load is fully isolated from any voltage phenomena that can occur at the grid delivery point. Since all the power supplied to the load flows through the UPS converters, this type of system provides also great control over the absorbed current. Therefore, the UPS can be regulated to absorb power with power factor close to the unit (independently from the load type and range). This type of UPS is the most used in medium and high-power applications. The present market solutions have power ratings reaching several MVA with efficiency up to 96.5 % [30].

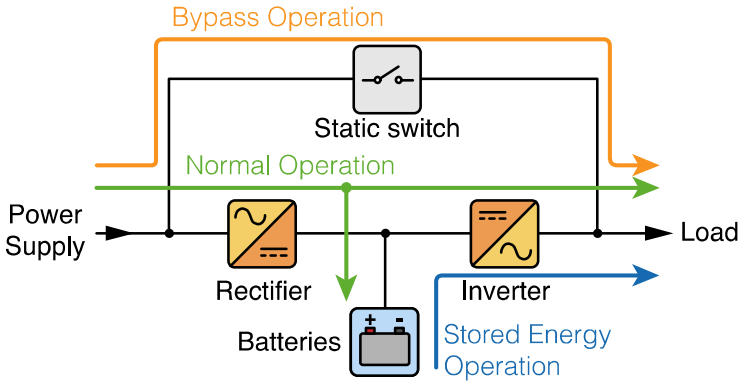



Figure 2.8: Typical configuration of a double-conversion UPS [2].

### 2.3.2 Control strategies for parallel-connected UPSs

The main UPS load-sharing control schemes available in the literature are shown in Figure 2.9. Two main groups can be defined depending on the presence or not of intercommunication between the paralleled UPS. If controllers of each UPS share information, the control scheme is defined as *active current-sharing* scheme. Otherwise, if no communication is required between the controllers, the control scheme is classified as *independent* (or *autonomous*). The main objective of the major part of such studies is to develop a strategy that ensures equal load current distribution between the paralleled UPS systems to naturally avoid potential circulating currents and equally distribute stress.

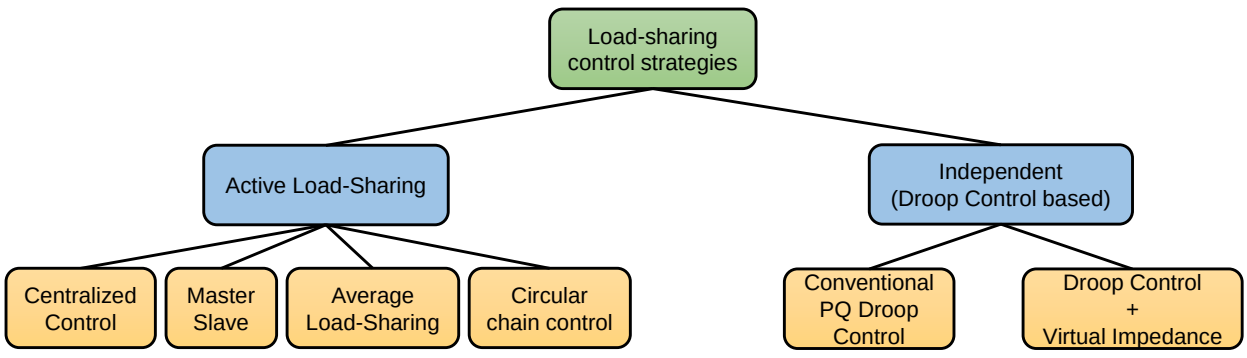



Figure 2.9: Main types of load-sharing control schemes used for paralleled connected UPS (adapted from [31] and [32]).

The active load-sharing methods are classified into four distinct groups:

- **Centralized Control**: In this type of control, the load voltage and the total load current are measured and sent to a centralized controller. In the centralized controller, there is an outer voltage control loop that generates a current reference based on the voltage error. This reference is then divided by the number of paralleled systems and sent to their respective controllers. To track this current reference, a current control loop is used locally in each UPS controller. This control scheme is usually adopted when a high number of UPSs are locally connected in parallel. Since the total load current needs to be measured, some limitations might exist in distributing the paralleled systems over a large area, using this type of control [33, 34].

- **Master-Slave (MS)**: In this control scheme, the controller of an UPS is defined as the master. The master controller uses a voltage control loop to regulate the load voltage by generating a current reference for its own (having into account the number of paralleled units). The master controller also contains a current control loop to track the generated reference current. The current that the master is providing to the load is used as the reference for the slaves, ensuring equal load-sharing. Some variants of this control scheme can be found in the literature mainly depending on the criteria used to choose the master controller. However, despite this selection criteria, usually, if the master module fails, another module is selected, ensuring that the load voltage keeps following the voltage reference. This type of control is often adopted for paralleled UPSs that are located inside the same rack [35–40].

- **Average Load-Sharing**: In this type of control, a democratic concept is adopted. All the output currents are measured and an average current value is computed. Each module must track the computed average value. A voltage control loop exists inside each UPS controller and the voltage reference is generated inside each UPS controller. For this type of control, a synchronization bus is required to ensure that the the voltage reference is exactly the same in the paralleled systems. Due to its democratic concept, this technique is highly reliable, modular and expandable [41–46].

- **Circular Chain Control**: In this type of control, the current reference for the first UPS is directly obtained from the measurement of the current of last UPS system and so on, creating a circular chain connection [47–49]. A variant of this control scheme is the current limitation control technique, in which a master-slave based architecture is adopted [48]. In this technique with exception of the master UPS controller (that controls the load voltage), the current reference of the slaves UPS controllers are generated and limited by the respective preceding module.

The independent control scheme, also known as autonomous or wireless control, avoids critical communication links which can improve the overall system reliability and decrease

the restrictions in the UPSs locations. The concept of this kind of control is very similar to a control scheme used in large-scale power systems, for controlling the power that a generator injects into the grid: by controlling the amplitude and phase difference between the inverter voltage and the load voltage the reactive and active power supplied by the paralleled systems are controlled (Conventional PQ droop control). The power supplied by each UPS is measured and interpreted by the controller of the respective UPS. Each UPS has its own voltage reference, whereby accordingly to the measured power, adjustments in those voltage references are made in order to change the power supplied by each UPS. The conventional PQ control scheme shows good performance if the output impedance of the system is predominantly inductive [50, 51] (which is the case of the generators in large-scale power systems).

Since a UPS system can also feed other types of loads, the load-sharing accuracy is in some cases significantly compromised. Therefore, control strategies consisting on the conventional droop method with an additional *virtual impedance loop* have been proposed [52–55]. By using a virtual output impedance loop in the control scheme, the voltage reference calculated by conventional droop method is following modified according to the feedback information introduced by this loop. In the loop, a transfer function to represent the virtual output impedance is used. Therefore by changing this transfer function accordingly to the connected load, a more precise load-sharing strategy is obtained. Even so, given the fact that in a UPS the load is typically unknown and can abruptly change, some limitations in defining a precise virtual impedance transfer function might arise.

In the *independent* control strategies, since the load voltage references are controlled to achieve load-sharing, a tradeoff between a precise load power distribution and a high-quality load voltage waveform typically exist.

## 2.4 Structure of the adopted system

Given the degree of protection that a *double conversion* UPS can provide to the load, it is the UPS type used in this work. Figure 2.10 illustrates the adopted system. Each UPS contains two 3-Level Neutral Point Clamped converters in a back-to-back configuration and two types of filters. For the grid-side an inductive filter is adopted, whereas for the load-side a LC filter is used. Since the UPS batteries and the DC-DC converter do not have any influence in the ZSCC circulation and in the proposed load-sharing technique, they are not considered in this work.

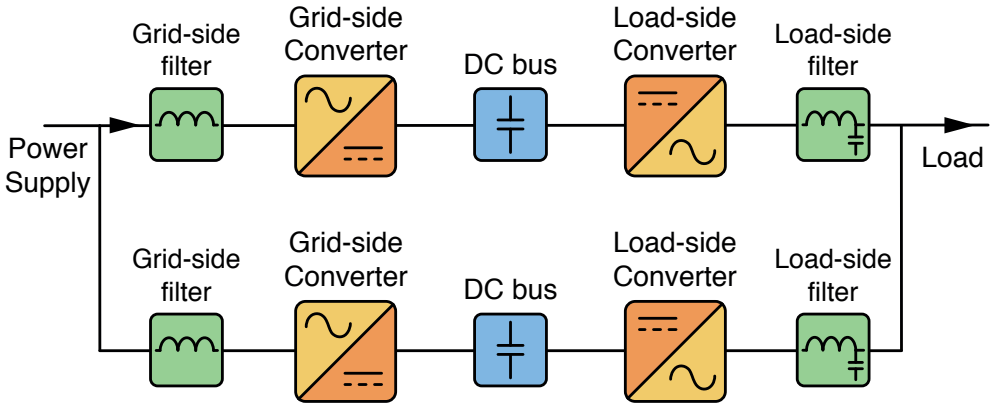



Figure 2.10: Adopted parallel connected system configuration.

# Chapter 3

# Control strategy

## 3.1 Mathematical model

The detailed circuit configuration of the adopted system is presented in Figure 3.1. The measured signals are represented in red. Each UPS system contains a grid-side converter (GSC) and a load-side converter (LSC) that share a double capacitor DC bus. As already mentioned, since the UPS batteries and the DC-DC converter do not have any influence in the ZSCC circulation and in the load-sharing strategy, they are not considered. The GSCs are connected to the grid using an inductive filter while the LSCs are connected to the load through an LC filter.

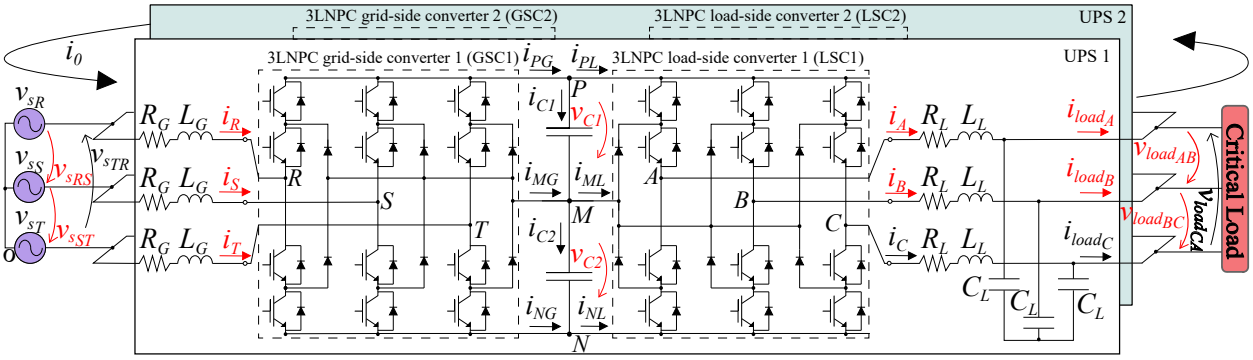



Figure 3.1: Circuit diagram of the proposed paralleled system.

The adopted 3LNPC topology contains 3 legs, each of them associated to a given phase $X$. For the GSC $X = \{R, S, T\}$, whereas for the LSC $X = \{A, B, C\}$. Each leg contains 4 IGBTs (with anti-parallel diodes), and 2 clamping diodes. For each phase there are three distinct switching states, leading to three different pole voltage values as Tab. 3.1 shows. The pole voltage $v_{XM}$ corresponds to the voltage between the AC terminal of phase $X$ and the middle point $M$ of the DC bus. Therefore, the 3LNPC converter has 27 possible switching states. Usually, to simplify the control of a converter, 3-phase variables are transformed to

Table 3.1: Switching states in phase $X$.

| Switching State ($S_X$) | Active IGBTs | Generated Pole Voltage ($v_{XM}$) |
|---|---|---|
| 1 | Upper two | $v_{C1}$ |
| 0 | Middle two | 0 |
| -1 | Lower two | $-v_{C2}$ |

space vector form. Regarding the GSC, such transformation is given by

$$\overline{x} = \frac{2}{3}(x_R + ax_S + a^2 x_T) = x_\alpha + jx_\beta \ , \tag{3.1}$$

where $a = e^{j\frac{2\pi}{3}}$ represents the space rotation coefficient and $\overline{x}$ represents the space vector. The LSC variables are transformed analogously.

### 3.1.1 Grid-side converter

The inductive filter that connects the GSC AC side to the grid was chosen to ensure appropriated current filtering without compromising the dynamic response of the converter. The GSC DC side is connected to the DC bus. From Figure 3.1 the following voltage equation can be written

$$v_{s_X} = L_G \frac{di_X}{dt} + R_G i_X + v_{XM} - v_{OM} \ . \tag{3.2}$$

The term $v_{s_X}$ corresponds to the grid phase voltage which is calculated from the measured line voltages. The term $i_X$ corresponds to the grid current. The term $v_{OM}$ corresponds to the converter Common Mode Voltage (CMV). The $O$ point corresponds to the neutral grid point. The CMV is deduced from (3.2), and is given by

$$v_{OM} = \frac{v_{RM} + v_{SM} + v_{TM}}{3} \ . \tag{3.3}$$

All three-phase signals are transformed to vector form. This removes the CMV component, simplifying the converter control. Therefore, equation (3.2) can be rewritten as

$$\overline{v}_s = L_g \frac{d\bar{i}_g}{dt} + R_g \bar{i}_g + \overline{v}_g \ . \tag{3.4}$$

where $\overline{v}_s$ is the grid voltage space vector, $\bar{i}_g$ is the grid current space vector and $\overline{v}_g$ is the converter voltage space vector.

From (3.4), the dynamics of the grid-side current is given by

$$\frac{d\bar{i}_g}{dt} = \frac{\overline{v}_s}{L_g} - \frac{R_g}{L_g}\bar{i}_g - \frac{\overline{v}_g}{L_g} \ . \tag{3.5}$$

The dynamics of DC bus capacitors voltage are defined as

$$\frac{dv_{C1}}{dt} = \frac{1}{C_{DC}} i_{C1} \ , \ \frac{dv_{C2}}{dt} = \frac{1}{C_{DC}} i_{C2} \ , \tag{3.6}$$

where the currents in the DC bus capacitors are given by $i_{C1} = i_{P_G} - i_{P_L}$ and $i_{C2} = i_{N_L} - i_{N_G}$. In these equations, $i_{P_G}$ and $i_{N_G}$ are the currents supplied to the DC bus by the GSC, whereas $i_{P_L}$ and $i_{N_L}$ are the currents absorbed by the LSC. The capacitance of each DC bus capacitor is the same and is given by the term $C_{DC}$. The currents absorbed by the DC bus are given by

$$\begin{aligned} i_{P_G} &= i_R \ (S_R = 1) + i_S \ (S_S = 1) + i_T \ (S_T = 1) \\ i_{M_G} &= i_R \ (S_R = 0) + i_S \ (S_S = 0) + i_T \ (S_T = 0) \\ i_{N_G} &= i_R \ (S_R = \text{-}1) + i_S \ (S_S = \text{-}1) + i_T \ (S_T = \text{-}1) \ , \end{aligned} \tag{3.7}$$

where $(S_X = s)$ is 1 if $S_X$ has value $s$ and 0 otherwise. The currents $i_{P_L}$, $i_{M_L}$ and $i_{N_L}$ are obtained analogously.

### 3.1.2 Load-side converter

The LSC DC side is connected to the DC bus, whereas the AC side is connected to the load through an LC filter that ensures high quality in output voltage waveform. Similarly to the mathematical model deduction made for the GSC, the following phase voltage equation can be written for the LSC

$$v_{load_X} = -L_L \frac{di_X}{dt} - R_L i_X + v_{XM} - v_{O'M} \ , \tag{3.8}$$

where the term $v_{load_X}$ is the load phase voltage which is calculated from the measured line voltages. The term $i_X$ corresponds to the LSC output current. The terms $v_{XM}$ and $v_{O'M}$ are respectively the pole voltage and CMV of the LSC, being O' in this case a fictitious neutral load point. The current $i_X$ is given by

$$i_X = i_{load_X} + i_{C_{L_X}} = i_{load_X} + C_L \frac{dv_{load_X}}{dt} \ . \tag{3.9}$$

In vector form, (3.8) and (3.9) are given respectively by

$$\overline{v}_{load} = -L_L \frac{d\overline{i}_L}{dt} - R_L \overline{i}_L + \overline{v}_L \ , \tag{3.10}$$

$$\overline{i}_L = \overline{i}_{load} + C_L \frac{d\overline{v}_{load}}{dt} \ . \tag{3.11}$$

Hence, the voltage and current dynamics are given by

$$\frac{d\overline{i}_L}{dt} = -\frac{1}{L_L} \overline{v}_{load} - \frac{R_L}{L_L} \overline{i}_L + \frac{1}{L_L} \overline{v}_L \ , \tag{3.12}$$

$$\frac{d\bar{v}_{load}}{dt} = \frac{1}{C_L}\bar{i}_L - \frac{1}{C_L}\bar{i}_{load} \tag{3.13}$$

### 3.1.3 Circulating current analysis

In a three-phase three-wire system, the sum of the phase currents is always zero. This is valid to the case in which a single three-wire UPS supplies a critical load. However, when the UPSs are connected in parallel, internal closed paths are formed accordingly to the different switching states applied to the converters of the two systems. Figure 3.2 shows an arbitrary moment during the system operation in which the circulating current is being formed. As it can be seen, all the converters have different switching states applied. In this case, the circulating current in all the three-phases have the same direction. It can be seen that the voltage sources that create these currents are the DC buses of each UPS. The circulating current in phase $R$ (represented in red) is during the given switching states only generated by the DC bus of UPS1, whereby in the phase $S$ and phase $T$ (represented in green and blue, respectively), the circulating current is generated by the voltages of the two DC buses (note that due to the converters switching states applied in phase $S$ and $T$ the DC buses are in series from the point of view of these phases). Since the high voltages of the DC buses are only applied to the inductors of the grid and load side filters, very low impedance paths are formed, leading to high circulating currents. Therefore, the circulating currents dynamics relies on the voltages of the DC buses, switching states of the converters (which can be quantified as the CMV generated by each converter as it will be seen bellow) and on the impedance of the filters.

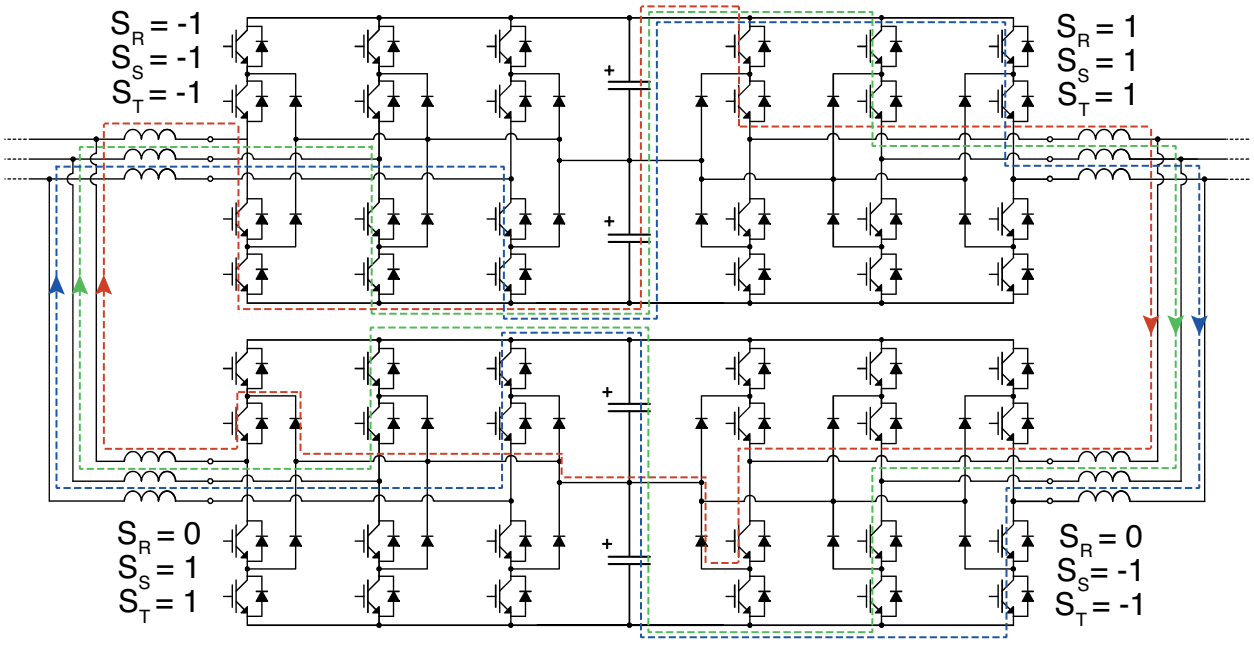



Figure 3.2: Circulating current generation example.

As it was seen, the current of each phase will have a DC (or zero harmonic) current component created by the DC buses. Therefore, in general, the literature designates the circulating current that exists in a paralleled power electronics system as a zero sequence circulating current (ZSCC). From the point of view of a UPS system controller, the ZSCC that circulates between the UPS systems through the connection points, can be detected by adding the phase currents at any point of the paralleled system. To obtain this current, instead of only two currents, the three grid currents of each UPS are measured. The ZSCC is given by

$$i_0 = \frac{i_R + i_S + i_T}{3} \,. \tag{3.14}$$

Similarly to the ZSCC dynamics analysis given in [56] for the parallel of two 3-Level T-type inverters, the following equation was obtained to study the dynamics of ZSCC in the paralleled UPSs

$$\frac{di_0}{dt} = \frac{3}{2} \cdot \frac{(v_{OM_{G2}} - v_{O'M_{L2}} + v_{O'M_{L1}} - v_{OM_{G1}})}{(R_G + R_L + L_G + L_L)} \,. \tag{3.15}$$

In this equation $v_{OM_{G2}}$, $v_{O'M_{L2}}$, $v_{O'M_{L1}}$, $v_{OM_{G1}}$ are the CMV of each converter, calculated using (3.3). The chosen convention for the positive direction of ZSCC is depicted in Figure 3.1. From (3.15) it can be seen that ZSCC dynamics highly depends on the linear combination of CMV of all the converters. Thus, by controlling the CMV generated by the converters, the ZSCC can be suppressed.

## 3.2 Proposed FCS-MPC controller

The control principle is the same for the two paralleled UPS. Therefore, the control scheme explained in this section is valid for both paralleled systems, expect when otherwise specified. As it will be seen in Chapter 4, each UPS system is controlled by the same controller. However, part of the control algorithm (regarding ZSCC suppression) was developed having in mind a future implementation of the control scheme in two independent control platforms. As proposed in [2, 1], a cooperative control strategy is adopted. The control action regarding the LSC is the first to be calculated. This means that the LSC switching state is chosen having into account only its effect in the respective UPS system. However, to choose the switching state to apply on the GSC, the controller takes into account the switching state already chosen for the LSC.

### 3.2.1 Controller delay compensation

In spite of the remarkable increase in processing capabilities of digital controllers, it is still impossible to acquire data, process it and output control decision almost instantaneously. Therefore, as used in [57–60, 1], a delay of one sample is considered between signal measure-

ment and the corresponding control action as Figure 3.3 demonstrates. All required signals are measured at $k$. Then, system state at $k+1$ is predicted, considering the previously chosen control action (applied at $k$). Finally the system state at $k+2$ is predicted for all possible switching states and the one that minimizes the cost function is selected and applied at $k+1$.

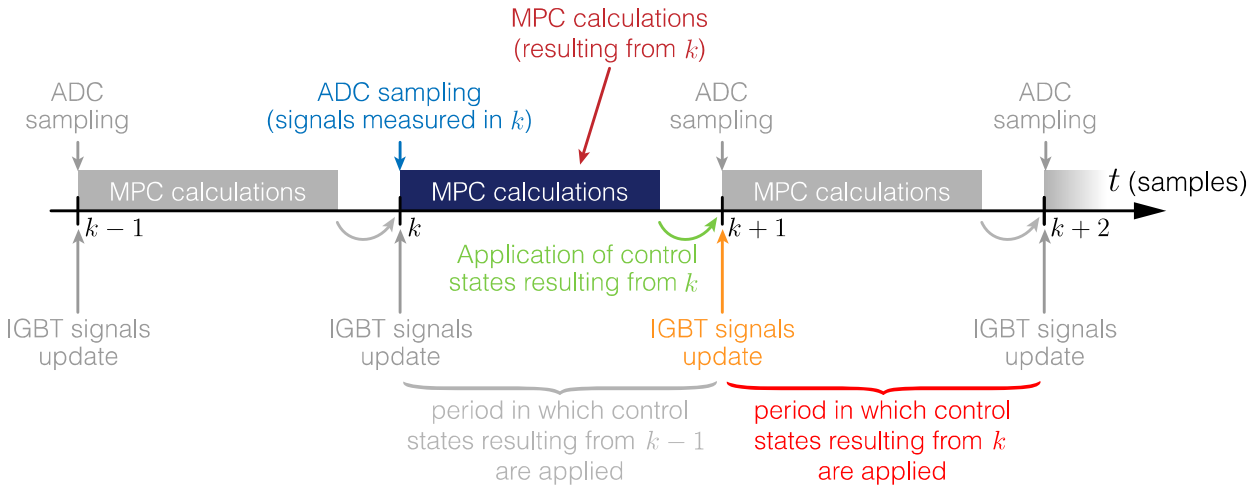



Figure 3.3: Main tasks carried out in a controller during each sampling period (the colored processes are referred to sample $k$) [2].

### Model prediction at $k+1$

In order to discretize the model, the forward Euler approximation is used. Hence, from the mathematical model previously presented, all the control variables at $k+1$ are predicted using the following equations:

$$\overline{v}_s^p[k+1] = \overline{v}_s[k] \cdot e^{\frac{2\pi}{0.02}T_s}\,, \tag{3.16}$$

$$\overline{i}_g^p[k+1] = \left(1 - \frac{R_G T_s}{L_G}\right)\overline{i}_g[k] + \frac{T_s}{L_G}\overline{v}_s[k] - \frac{T_s}{L_G}\overline{v}_g[k]\,, \tag{3.17}$$

$$\overline{i}_L[k+1] = \left(1 - \frac{R_L T_s}{L_L}\right)\overline{i}_L[k] - \frac{T_s}{L_L}\overline{v}_{load}[k] + \frac{T_s}{L_L}\overline{v}_L[k]\,, \tag{3.18}$$

$$v_{C_n}^p[k+1] = v_{C_n}[k] + \frac{T_s}{C_{DC}} i_{C_n}[k] \quad , \quad n = \{1,2\}\,, \tag{3.19}$$

$$\overline{v}_{load}^p[k+1] = \overline{v}_{load}[k] + \frac{T_s}{C_{eq}}(\overline{i}_{C_{L_{(UPS1)}}}[k] + \overline{i}_{C_{L_{(UPS2)}}}[k])\,, \tag{3.20}$$

$$i_0^p[k+1] = i_0[k] + \frac{3T_s(v_{OM_{G2}} - v_{O'M_{L2}} + v_{O'M_{L1}} - v_{OM_{G1}})[k]}{2(R_G + R_L + L_G + L_L)}\,, \tag{3.21}$$

where $T_s$ is the control sampling time. In (3.20) the terms $\bar{i}_{C_{L_{(UPS1)}}}$ and $\bar{i}_{C_{L_{(UPS2)}}}$ are the space vector currents of the capacitors of each load-side filter, and are calculated using

$$\bar{i}_{C_{L_{(UPS1)}}} = \bar{i}_{L_{(UPS1)}} - \bar{i}_{load_{(UPS1)}} , \tag{3.22}$$

$$\bar{i}_{C_{L_{(UPS2)}}} = \bar{i}_{L_{(UPS2)}} - \bar{i}_{load_{(UPS2)}} . \tag{3.23}$$

### 3.2.2 Load-side current references calculation

Since both UPS systems are sharing the same load, at least one UPS controller must know the total load current. Thus, in the developed control scheme, the load current being supplied by LSC2 is sent to the LSC1 controller. Independently of the power distribution between systems, the load voltage must follow a sinusoidal voltage reference. Since a direct control of the load voltage does not allow a load-sharing strategy, this voltage is controlled through a control scheme based on direct current control. An equivalent output capacitor filter is defined as $C_{eq} = 2 \cdot C_L$. The total current flowing in $C_{eq}$ is controlled, so that the load voltage follows the voltage reference. The percentage of power that each system supplies to the load is defined by controlling the current that each system injects into $C_{eq}$. The proportion of load power assigned to UPS1 is defined as $\lambda_1$, whereby the proportion of power supplied by UPS2 is given by $\lambda_2 = 1 - \lambda_1$. Using the backward Euler approach, the total current necessary in the equivalent capacitor to track the output voltage reference is given by

$$\bar{i}^*_{L_T}[k+2] = \bar{i}_{load_T}[k+2] + \frac{C_{eq}}{T_s}(\bar{v}^*_{load}[k+2] - \bar{v}^p_{load}[k+1]) , \tag{3.24}$$

where $\bar{i}^*_{L_T}[k+2]$ is the reference current vector, $\bar{v}^*_{load}[k+2]$ is the reference voltage vector and $\bar{i}_{load_T}[k+2]$ is the total load current. Finally, the current references for each UPS system are given by

$$\bar{i}^*_{L1}[k+2] = \lambda_1 \cdot \bar{i}^*_{L_T}[k+2], \tag{3.25}$$

$$\bar{i}^*_{L2}[k+2] = \lambda_2 \cdot \bar{i}^*_{L_T}[k+2]. \tag{3.26}$$

### 3.2.3 Grid-side current references calculation

The developed control scheme for GSC control is based on the conventional control strategy presented in [1].

The grid current reference calculation is based on the active power balancing in each UPS. Instead of considering instantaneous power values, the average power is considered. Thus, high variations in the load within a fundamental period are overlooked leading to more stable absorbed currents. Figure 3.4 shows the power flow in each UPS system.

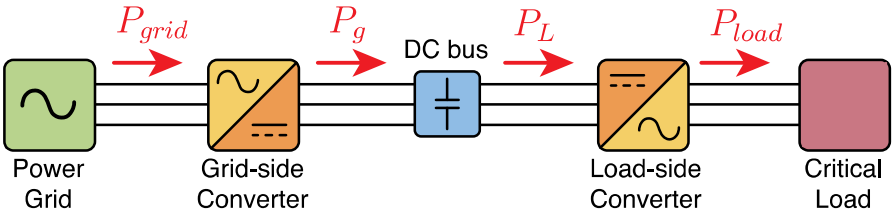



Figure 3.4: Power flow in a single UPS system [2].

The power balancing in one system can be written as

$$P^*_{grid} = (P_{grid} - P_g) + P_L + P^*_{charge}\,, \tag{3.27}$$

where, $P^*_{grid}$ corresponds to the reference active power to be drawn from the grid; $P_{grid}$ is the power actually drawn from the grid; $P_G$ is the power supplied by the grid-side converter to the DC bus; $P_L$ is the power drawn from DC bus by the LSC. The difference $P_{grid} - P_g$ represents the losses in the GSC. Finally, the term $P^*_{charge}$ corresponds to the power necessary to charge/discharge the DC bus from its current voltage to its reference voltage. These terms can be calculated using the following equations:

$$P_g = \frac{1}{T}\int_0^T v_{C_1} \cdot i_{P_g} - v_{C_2} \cdot i_{N_g}\, dt\,, \tag{3.28}$$

$$P_L = \frac{1}{T}\int_0^T v_{C_1} \cdot i_{P_L} - v_{C_2} \cdot i_{N_L}\, dt\,, \tag{3.29}$$

$$P_{grid} = \frac{3}{2}\frac{1}{T}\int_0^T v_{s_\alpha} \cdot i_{g_\alpha} - v_{s_\beta} \cdot i_{g_\beta}\, dt\,. \tag{3.30}$$

In the controller, these terms are actually calculated using discrete-time integration. To compute $P_{grid}$, the correcting factor 3/2 is required since the amplitude-invariant Clark transform is used to obtain the $\alpha\beta$ components of voltages and currents. To calculate the $P^*_{charge}$ term, the required energy to charge/discharge the capacitors needs to be calculated first. Since the energy in a DC bus capacitor is given by

$$E_{C_1} = \frac{1}{2} \cdot C_{DC} \cdot v^2_{C_1}\,, \tag{3.31}$$

$$E_{C_1} = \frac{1}{2} \cdot C_{DC} \cdot v^2_{C_1}\,, \tag{3.32}$$

the total required energy is given by

$$E_{charge} = 2 \cdot \frac{1}{2} \cdot C_{DC} \cdot \left(\left(\frac{v^*_{DC}}{2}\right)^2 - \left(\frac{v_{DC}}{2}\right)^2\right) = \frac{1}{4} \cdot C_{DC} \cdot (v^{*2}_{DC} - v^2_{DC})\,, \tag{3.33}$$

where $C_{DC}$ represents the capacitance of one DC bus capacitor. The term $v^*_{DC}$ is the DC bus voltage reference and $v_{DC}$ is the measured bus voltage. Finally, the term $P^*_{charge}$ is given by

$$P^*_{charge} = \frac{C_{DC} \cdot (v^{*2}_{DC} - v^2_{DC})}{4 \cdot T_s \cdot N_{th}} \,. \tag{3.34}$$

To limit the currents drawn by the GSC, a time horizon of $N_{th}$ samples is adopted.

Figure 3.5 shows a representation of the grid references calculation. The amplitude and

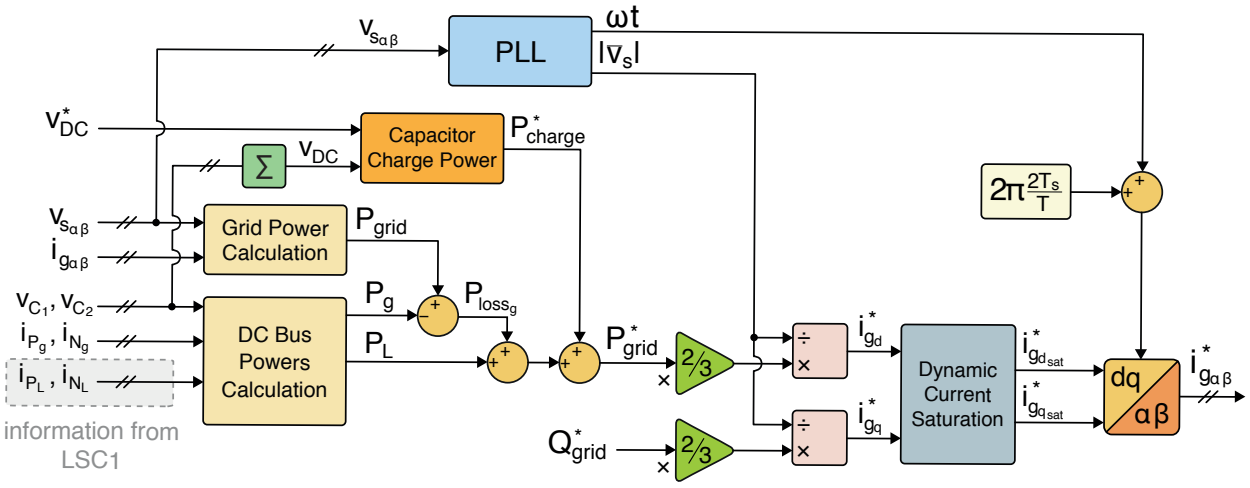



Figure 3.5: Schematic of the GSC1 current references calculation (adapted from [2]).

phase of grid voltage vector ($|\overline{v}_s|$ and $\angle\overline{v}_s$) are obtained using a Phase-Locked Loop (PLL). The term $Q^*_{grid}$ is the target reactive power to be absorbed from grid. Usually, this term is desired to be null, however in specific cases, as for PF correction, it can be regulated into a certain value. The current references are firstly calculated in the $dq$ rotating frame using the power reference and the grid voltage vector amplitude given by the PLL. To protect the GSC, it is of prompt importance that the reference currents do not surpass a maximum value. A dynamic saturation process is adopted to limit the $dq$ calculated references. The saturated currents in the $dq$ are frame given by:

$$i^*_{g_{d_{sat}}} = \begin{cases} i^*_{g_{max}} \cdot sign(|i^*_{g_d}|), & |i^*_{g_d}| > i_{g^*_{max}} \\ i^*_{g_d}, & otherwise \end{cases} \tag{3.35}$$

$$i^*_{g_{d_{sat}}} = \begin{cases} 0, & |i^*_{g_d}| > i_{g^*_{max}} \\ \sqrt{i^{*2}_{g_{max}} - i^{*2}_{g_d}}., & |i^*_{g_d}| \leqslant i_{g^*_{max}} \wedge |i^*_{g_d} + j \cdot i^*_{g_q}| > i_{g^*_{max}} \\ i^*_{g_q}, & otherwise \end{cases} \tag{3.36}$$

Finally, the $dq$ saturated references are transformed to $\alpha\beta$ components using the following equation

$$\overline{i}_g^*[k+2] = i_{g_\alpha}^*[k+2] + j \cdot i_{g_\beta}^*[k+2] = (i_{g_{d_{sat}}}^* + j \cdot i_{g_{q_{sat}}}^*) \cdot e^{j(\angle \overline{v}_s + 2\pi \frac{2T_s}{0.02})} , \tag{3.37}$$

where the constant $2\pi\frac{2T_s}{0.02}$ is added to $\angle\overline{v}_s$ in order to obtain the references at $k+2$.

### 3.2.4 Load-side controller

The FCS-MPC controller scheme adopted for the LSC1 is depicted in Figure 3.6. The LSC2 controller scheme is very similar (not represented to avoid redundancy). The big difference is the fact that the current references calculation block is only adopted in the LSC1 controller. Therefore, the load current references for the LSC2 are calculated in the LSC1. This way, it is ensured that the current references were calculated having into account the exact output voltage reference.

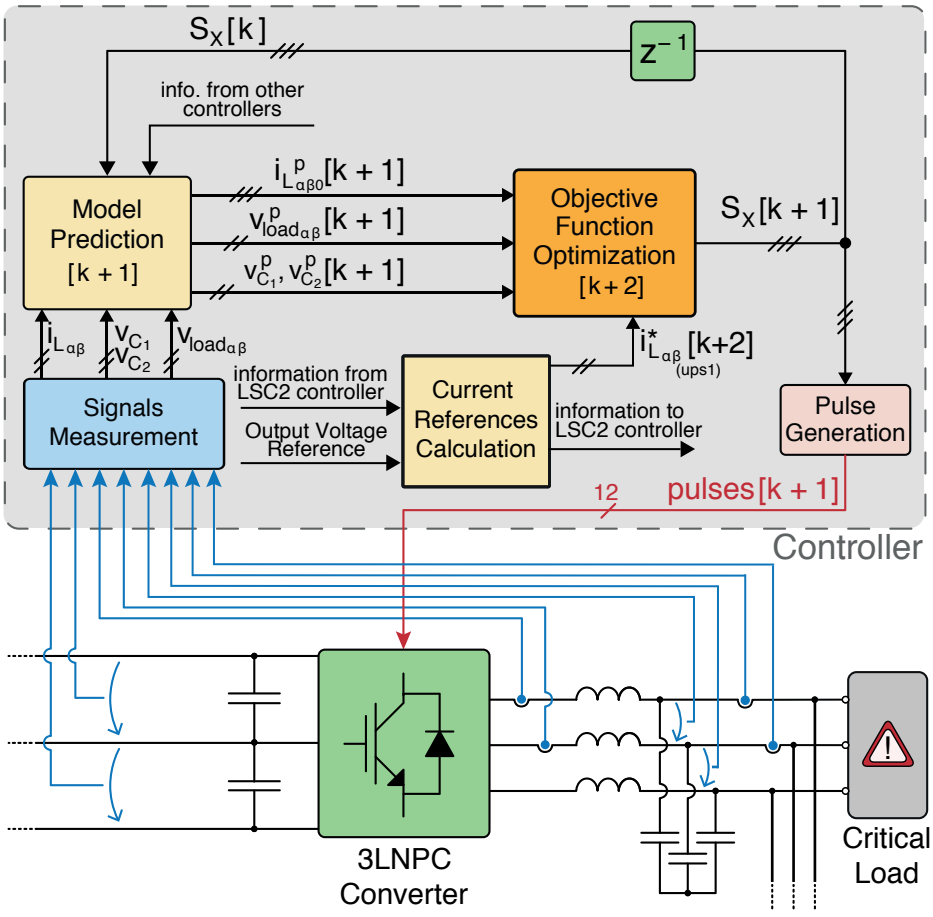



Figure 3.6: Representation of the FCS-MPC strategy implemented to the LSC1 (adapted from [2]).

### Objective function

Three objectives are considered regarding the LSC control:

1. Converter output current vector error minimization;
2. Minimization of DC bus capacitors voltage unbalance;
3. Minimization of the ZSCC.

The predicted output converter current at $k+2$ is given by

$$\overline{i}_L^p[k+2] = \overline{i}_L^p[k+1] - \frac{T_s}{L_L}\overline{v}_{load}^p[k+1] - \frac{T_s R_L}{L_L}\overline{i}_L^p[k+1] + \frac{T_s}{L_L}\overline{v}_L[k+1] \tag{3.38}$$

where $\overline{v}_L[k+1]$ corresponds to the converter voltage vector at $k+1$. This is the only variable term in the equation since it depends on the switching states being evaluated to be applied at $k+1$.

The DC bus capacitors unbalance at $k+2$ is given by:

$$\Delta v_{C_{1,2}}^p[k+2] = \Delta v_{C_{1,2}}^p[k+1] + \frac{T_s}{C_{DC}} i_{M_L}[k+1] \ , \tag{3.39}$$

where $\Delta v_{C_{1,2}}^p = v_{C1}^p - v_{C2}^p$.

As mentioned before, the proposed control strategy was developed, having into consideration a future implementation in two independent control platforms. Thus, due to limitations in real-time communication between independent control platforms of the UPSs, each controller only knows the switching states to be applied at $k+1$ in the converters of the respective UPS. The predicted ZSCC considered by the UPS1 and UPS2 controllers when computing control action for the respective LSCs are given by

$$i_{0_{L1}}^p[k+2] = i_0^p[k+1] + \frac{3T_s(v_{O'M_{L1}}[k+1])}{2(L_G + L_L + R_G + R_L)} \ , \tag{3.40}$$

$$i_{0_{L2}}^p[k+2] = i_0^p[k+1] + \frac{3T_s(-v_{O'M_{L2}}[k+1])}{2(L_G + L_L + R_G + R_L)} \ . \tag{3.41}$$

The partial objective functions regarding output current, DC bus capacitors unbalance and ZSCC are respectively given by

$$g_{i_L} = \sqrt{(i_{L_\alpha}^*[k+2] - i_{L_\alpha}^p[k+2])^2 + (i_{L_\beta}^*[k+2] - i_{L_\beta}^p[k+2])^2} \tag{3.42}$$

$$g_{bal_L} = |v_{C1}^p[k+2] - v_{C2}^p[k+2]| \tag{3.43}$$

$$g_{z_L} = |i_{0_L}^p[k+2]| \tag{3.44}$$

The global objective function regarding LSC control is given by

$$G_{LSC} = g_{i_L} \cdot W_{i_L} + g_{bal_L} \cdot W_{bal_L} + g_{z_L} \cdot W_{z_L}. \tag{3.45}$$

As shown in Figure 3.7, this equation is evaluated for the 27 possible combinations, and combines partial objective functions $g_x$ weighted by respective weights $W_x$, associated with each of the three objectives.

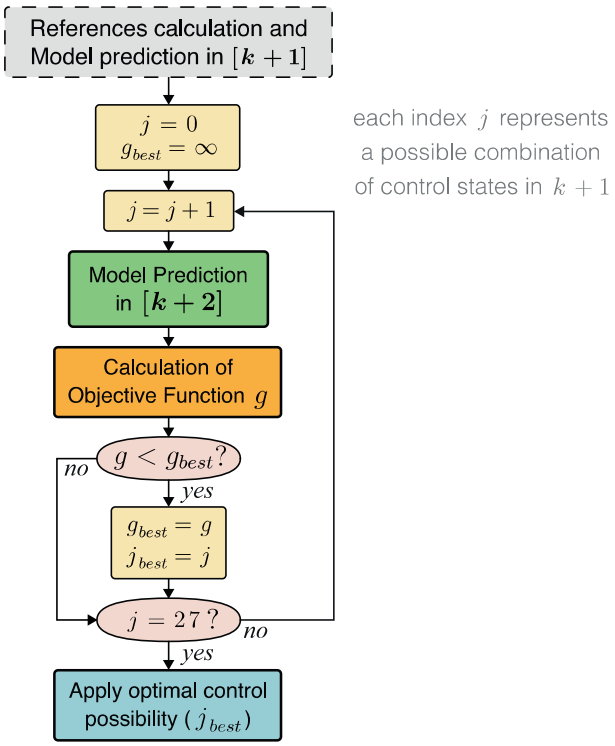



Figure 3.7: Flowchart regarding a cost function minimization [2].

### 3.2.5 Grid-side controller

The FCS-MPC controller scheme adopted for the GSC1 is depicted in Figure 3.8. In this case, the GSC2 controller scheme is exactly the same. Note that to calculate the grid current references, each GSC controller receives information from the LSC controller of the respective UPS.

#### Objective Function

Regarding the GSC control, three objectives are also considered:

1. Reference grid current vector tracking;
2. Minimization of DC bus capacitors voltage unbalance;

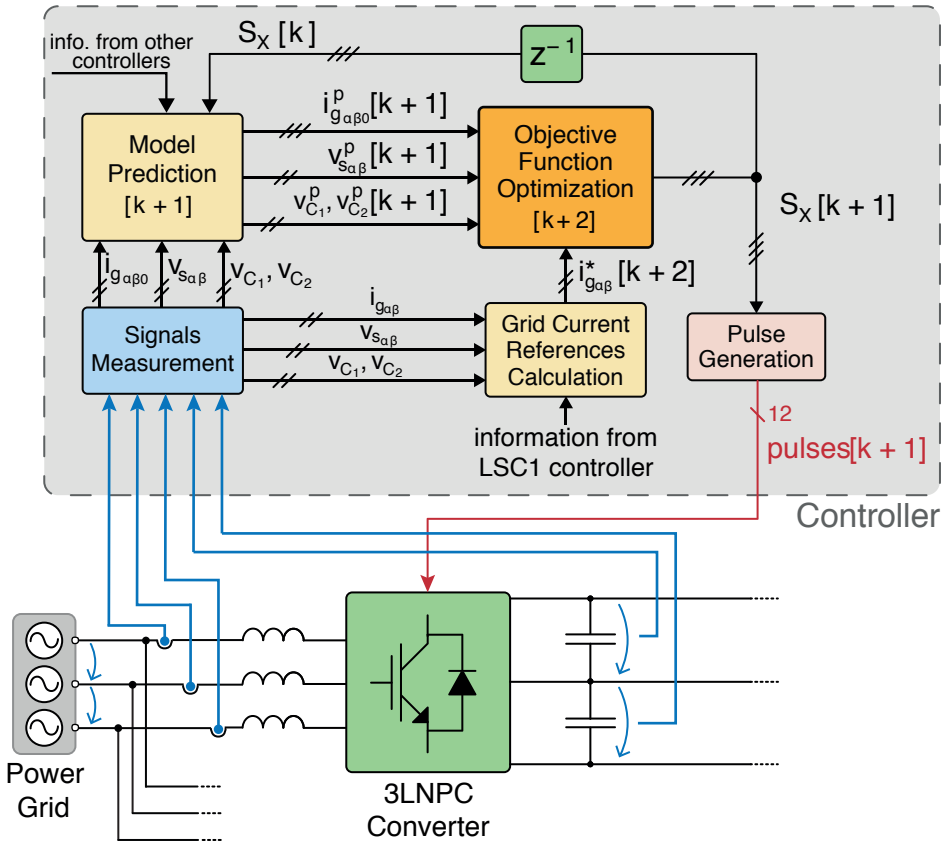



Figure 3.8: Representation of the FCS-MPC strategy implemented to the GSC1 (adapted from [2]).

3. Minimization of the ZSCC.

After the LSC controller is computed, the GSC objective function at $k+2$ can be evaluated.

The predicted grid current vector is given by

$$\overline{i}^p_g[k+2] = \overline{i}^p_g[k+1] - \frac{R_G T_s}{L_G}\overline{i}^p_g[k+1] + \frac{T_s}{L_G}\overline{v}^p_s[k+1] - \frac{T_s}{L_G}\overline{v}_g[k+1]\,. \tag{3.46}$$

The predicted DC bus capacitors unbalance is given by

$$\Delta v^p_{C_{1,2}}[k+2] = \Delta v^p_{C_{1,2}}[k+1] + \frac{T_s}{C_{DC}}\Big(i_{M_L}[k+1] - i_{M_G}[k+1]\Big)\,, \tag{3.47}$$

where the term $i_{M_L}[k+1]$ is previously calculated in the LSC controller. By introducing this term in the GSC objective function, the effect of the LSC on the capacitors unbalance is taken into consideration in the GSC controller.

The predicted ZSCCs considered by each controller to select the control action for the GSCs is given by

$$i^p_{0_{G1}}[k+2] = i^p_0[k+1] + \frac{3T_s(v_{O'M_{L1}}[k+1] - v_{OM_{G1}}[k+1])}{2(L_G + L_L + R_G + R_L)}, \tag{3.48}$$

$$i^p_{0_{G2}}[k+2] = i^p_0[k+1] + \frac{3T_s(v_{OM_{G2}}[k+1] - v_{O'M_{L2}}[k+1])}{2(L_G + L_L + R_G + R_L)}. \tag{3.49}$$

Since the control action to be taken by each LSC was already selected, its effect is also taken into account in the respective GSC ($v_{O'M_{L1}}$,$v_{O'M_{L2}}$).

Finally, the global objective function regarding GSC control is

$$G_{GSC} = g_{i_G} \cdot W_{i_G} + g_{bal_G} \cdot W_{bal_G} + g_{z_G} \cdot W_{z_G} \ . \tag{3.50}$$

where the terms $g_{i_G}$, $g_{bal_G}$ and $g_{z_G}$ are calculated analogously to (3.42), (3.43) and (3.44), respectively.

# Chapter 4

# Simulation Results and Experimental Validation

In this chapter, the simulation and experimental results of several tests are presented. For the simulation tests, the controllers were implemented in *Matlab/Simulink* environment. Figure 4.1 shows an illustration of the developed simulation model. Detailed information about this model can be found in Appendix A.

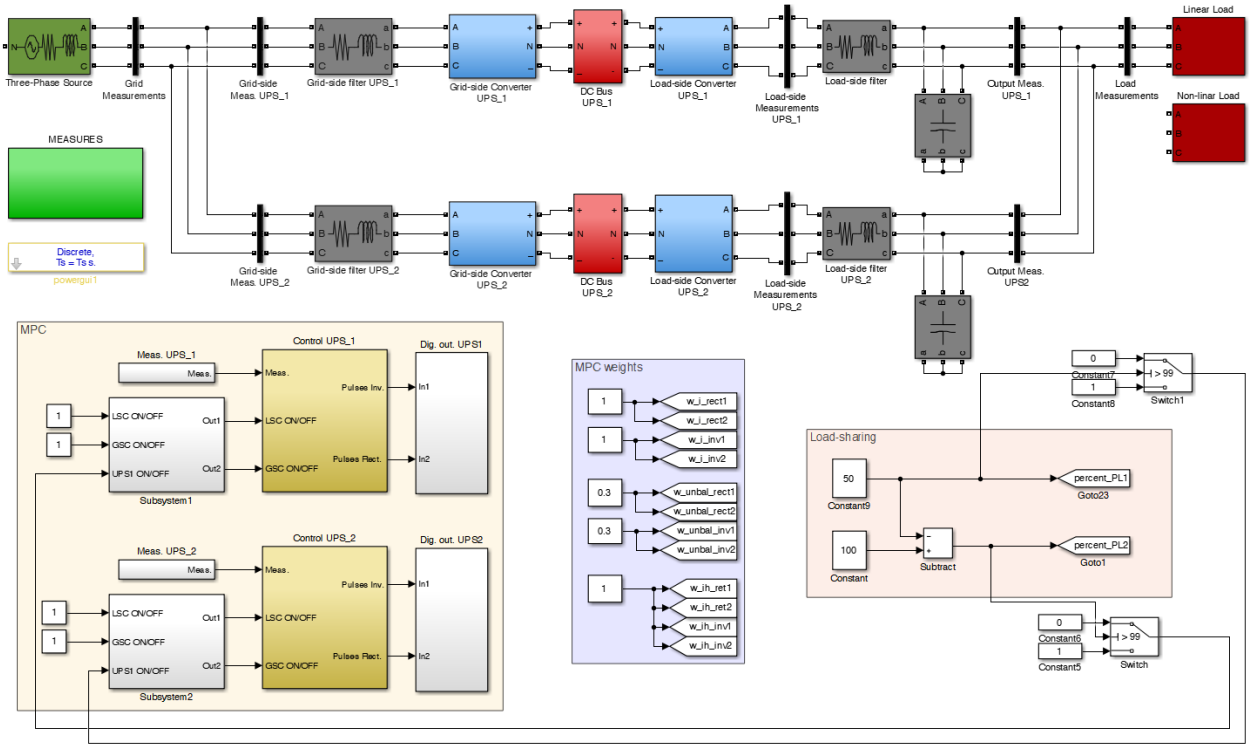



Figure 4.1: Developed simulation model implemented in *Matlab/Simulink*.

Figure 4.2 shows a schematic representation of the setup used for the experimental tests. Figure 4.3 shows a real labeled picture of the experimental setup.

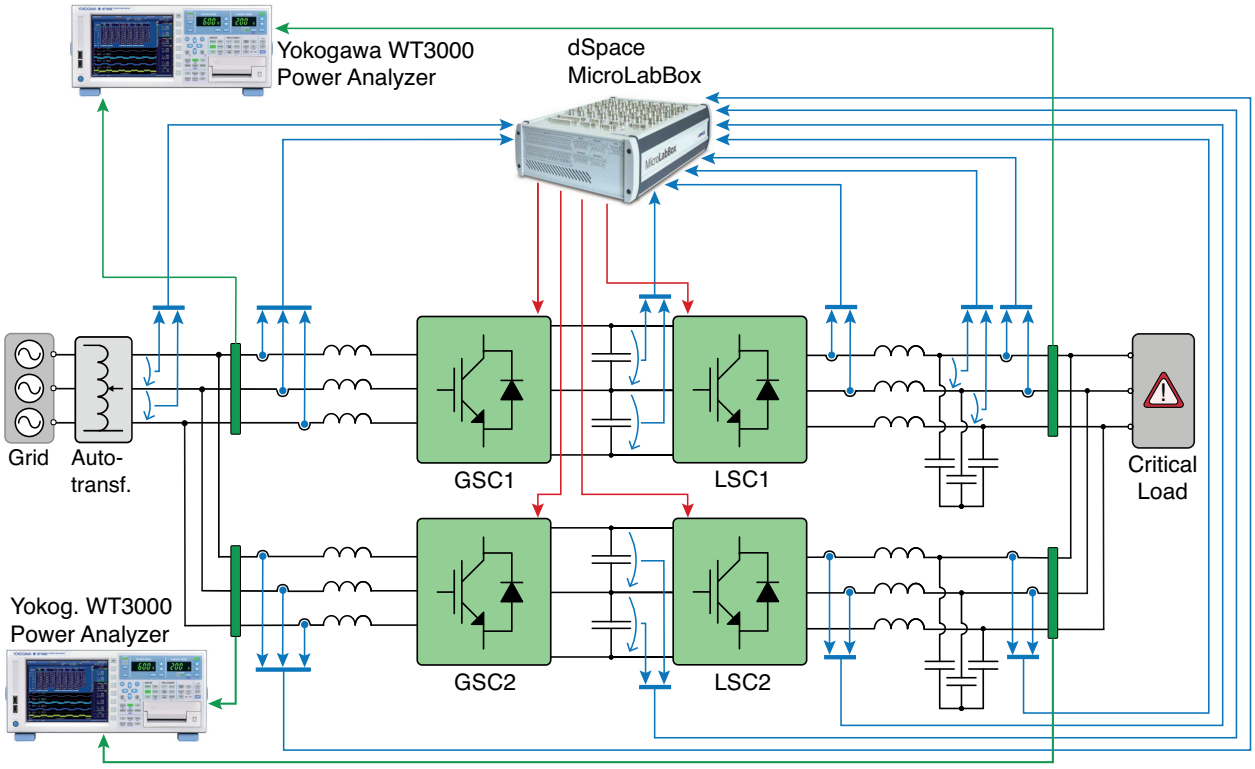



Figure 4.2: Schematic representation of the laboratory setup.

For the signals acquisition, control execution and IGBTs activation a *dSpace MicroLabBox* controller was used. To protect the controller, optical coupling was used for IGBTs activation. A sampling time of 70 $\mu$s was considered for all the controllers. For additional information about the used laboratory setup, reader should refer to Appendix B.

As Figure 4.4 shows, two types of loads were considered. A three-phase resistance was used as the linear load (R=50 $\Omega$), and a three-phase rectifier feeding an RC circuit as the non-linear load (R=50 $\Omega$, C=159$\mu$F). In Table 4.1 are listed the electrical parameters used either for the simulation and for the experimental tests. The control references and weighting factors[1] used in both UPSs controllers are listed in Table 4.2. Due to hardware limitations, two different inductances were used as grid-side filters, and the same is true for the load-side filters capacitors. Since some differences exist between the filters of each UPS, their individual performance feeding the critical load was tested.

The results presented in this chapter are organized as follows: firstly the individual performance of each UPS is studied. Then, the effectiveness of the control scheme in reducing the circulating current is assessed. Finally, the asymmetric load-sharing operation is presented.

[1]These weighting factors were chosen through empirical tests and are used in the controllers of both UPSs.

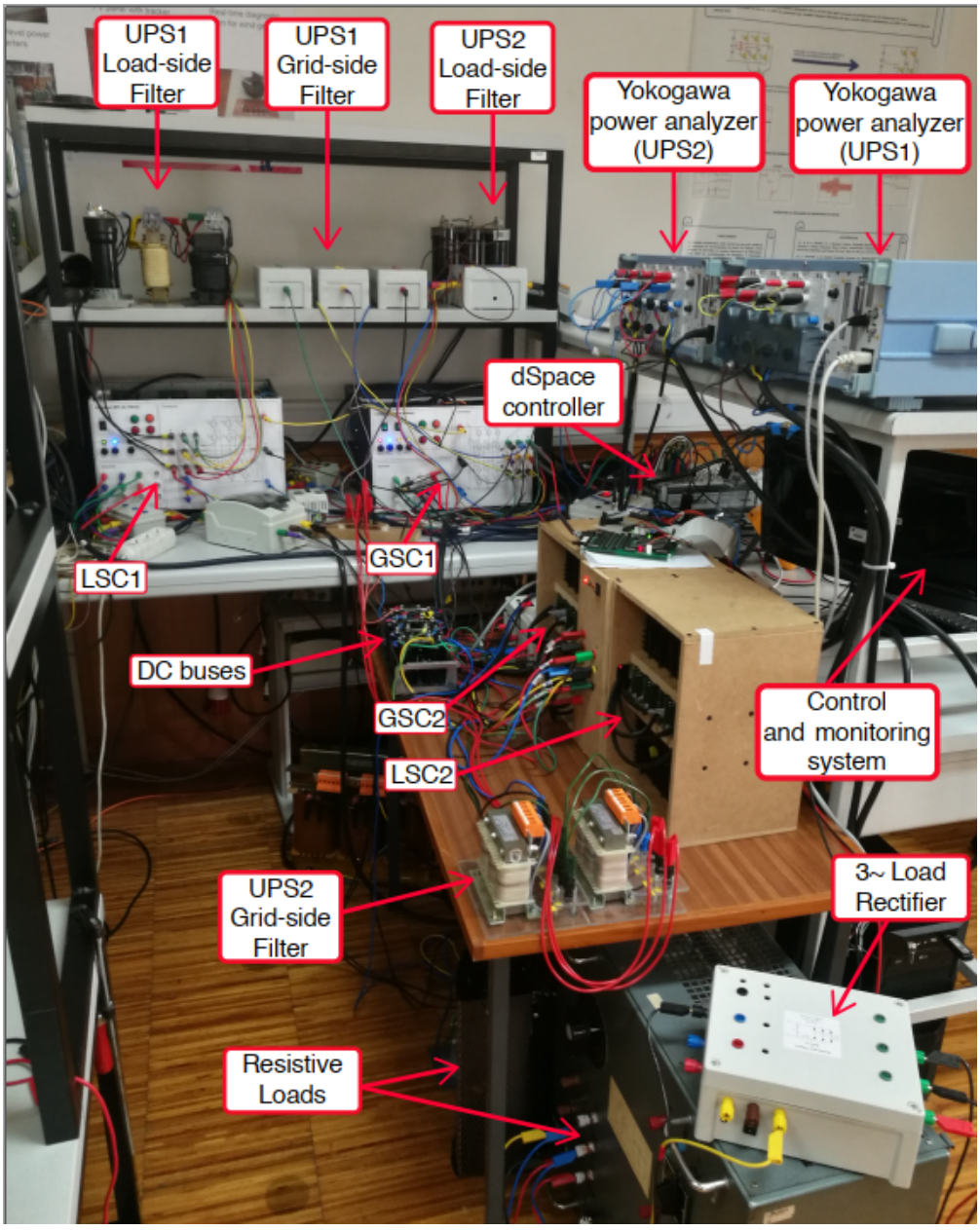



Figure 4.3: Experimental setup of the full system.

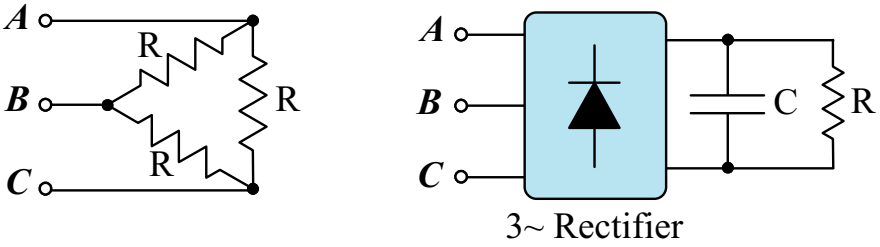



Figure 4.4: Types of critical loads used for the experimental tests.

Table 4.1: Electrical parameters of the simulation model and the experimental setup.

| Electrical Parameter | Value |
|---|---|
| Grid line voltage (RMS) | 120 V |
| Grid voltage frequency | 50 Hz |
| UPS1 grid-side filter | 13.5 mH |
| UPS2 grid-side filter | 5 mH |
| UPS1 and UPS2 DC bus capacit. | 3 mF |
| LSC1 and LSC2 filter inductance | 2.7 mH |
| LSC1 load-side filter capacitance | 66 $\mu$F |
| LSC2 load-side filter capacitance | 33 $\mu$F |

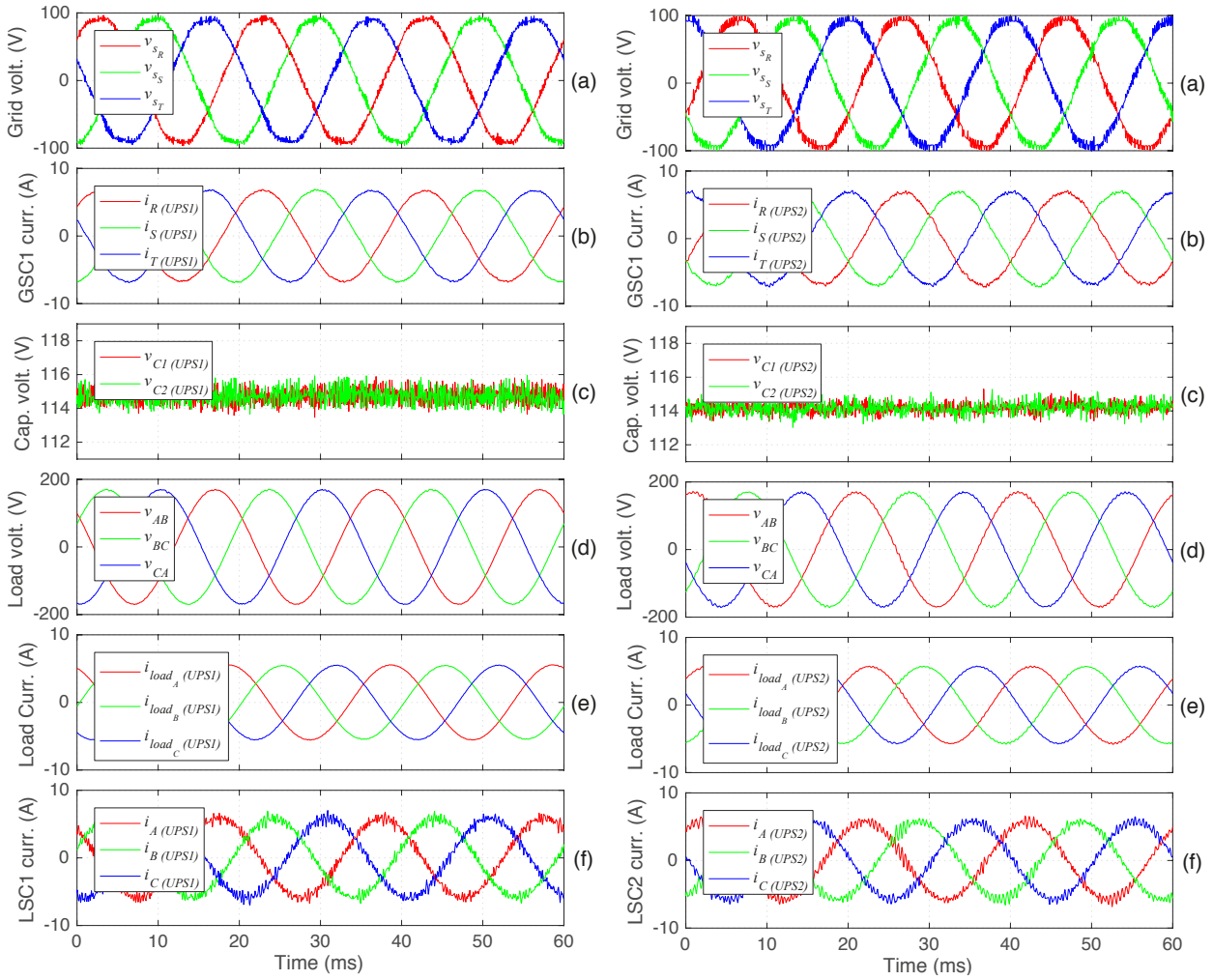
Table 4.2: Simulation and experimental control parameters.

| Control Parameter | Value |
|---|---|
| Load line voltage (RMS) | 120 V |
| Load voltage frequency | 50 Hz |
| DC charge horizon ($N_{th}$) | 500 |
| UPS1 and UPS2 DC bus voltage reference | 220 V |
| $W_{i_G}$, $W_{i_L}$, $W_{z_G}$ and $W_{z_L}$ | 1 |
| $W_{bal_G}$ and $W_{bal_L}$ | 0.3 |

## 4.1 Single UPS operation

A comparison between the performance of each UPS system is now presented. The UPS that is providing power to the load is fully isolated from the other. To avoid redundancy, only the experimental results are presented regarding isolated operation. Figure 4.5 shows the UPS1 and UPS2 performance feeding the linear load. Near sinusoidal currents are absorbed from the grid by each UPS. It can be seen that the grid-side currents of the UPS2 present slightly higher distortion due to a lower inductive filter. The load voltage generated by each UPS is practically sinusoidal. Since the load-side filter of the UPS2 has a lower capacitance compared to the load-side filter of the UPS1, the load voltage generated by the UPS2 is also slightly more distorted.

The DC bus voltage of each UPS is stable and the capacitors voltage balanced. However, an error of approximately 8 V can be observed in the voltage of the buses. This steady-state error is caused by inaccuracies in the calculation of the powers absorbed/supplied by each DC bus. These inaccuracies are mainly imposed by delays in IGBTs activation, deviations in




(a) Operation of the UPS1.

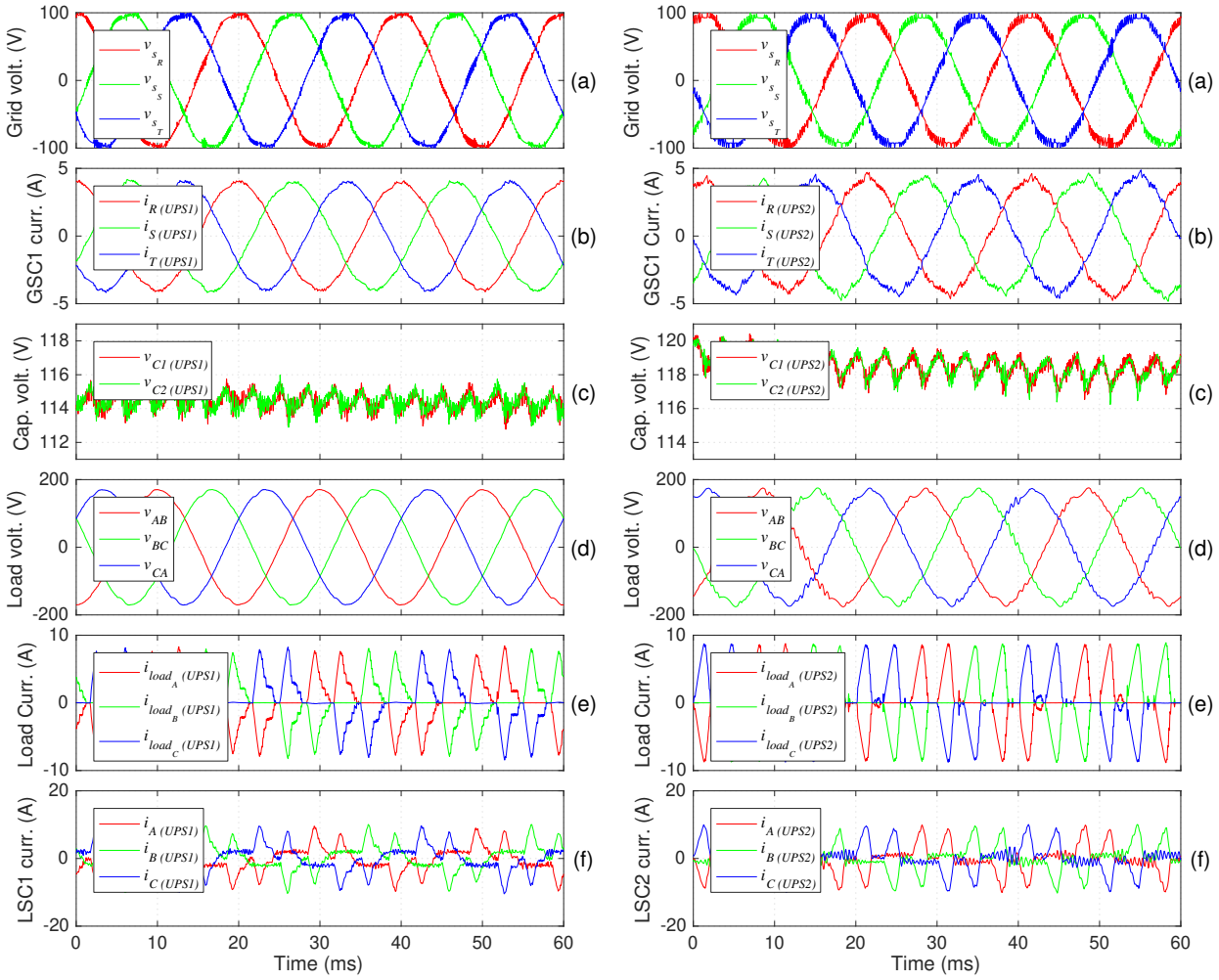
(b) Operation of the UPS2.

Figure 4.5: Individual UPS performance supplying a linear load (R=50 Ω) [Experimental].

the mathematical model and non-linearities in the circuit components. However, in terms of each UPS performance this deviation is absolutely negligible, and is therefore overlooked.

In Figure 4.6 the performance of each UPS feeding the non-linear load is presented. Since during a period the instantaneous power absorbed by the load has a non-linear behaviour, higher voltage ripple in the DC buses is observed. This could be avoided if a instantaneous power balancing was considered for the grid current references calculation. However, this approach would lead to highly distorted absorbed currents, which represents a much more undesirable situation. Due to its higher capacitive load-side filter, for a non-linear load, the UPS1 is capable of generating a load voltage waveform with considerably lower harmonic distortion than the UPS2 (1.47 % vs 7.73 %)[2].

[2]THD values provided by each power analyzer




(a) Operation of the UPS1.

(b) Operation of the UPS2.

Figure 4.6: Individual UPS performance supplying a non-linear load (R=50 Ω, C=159$\mu$F) [Experimental].

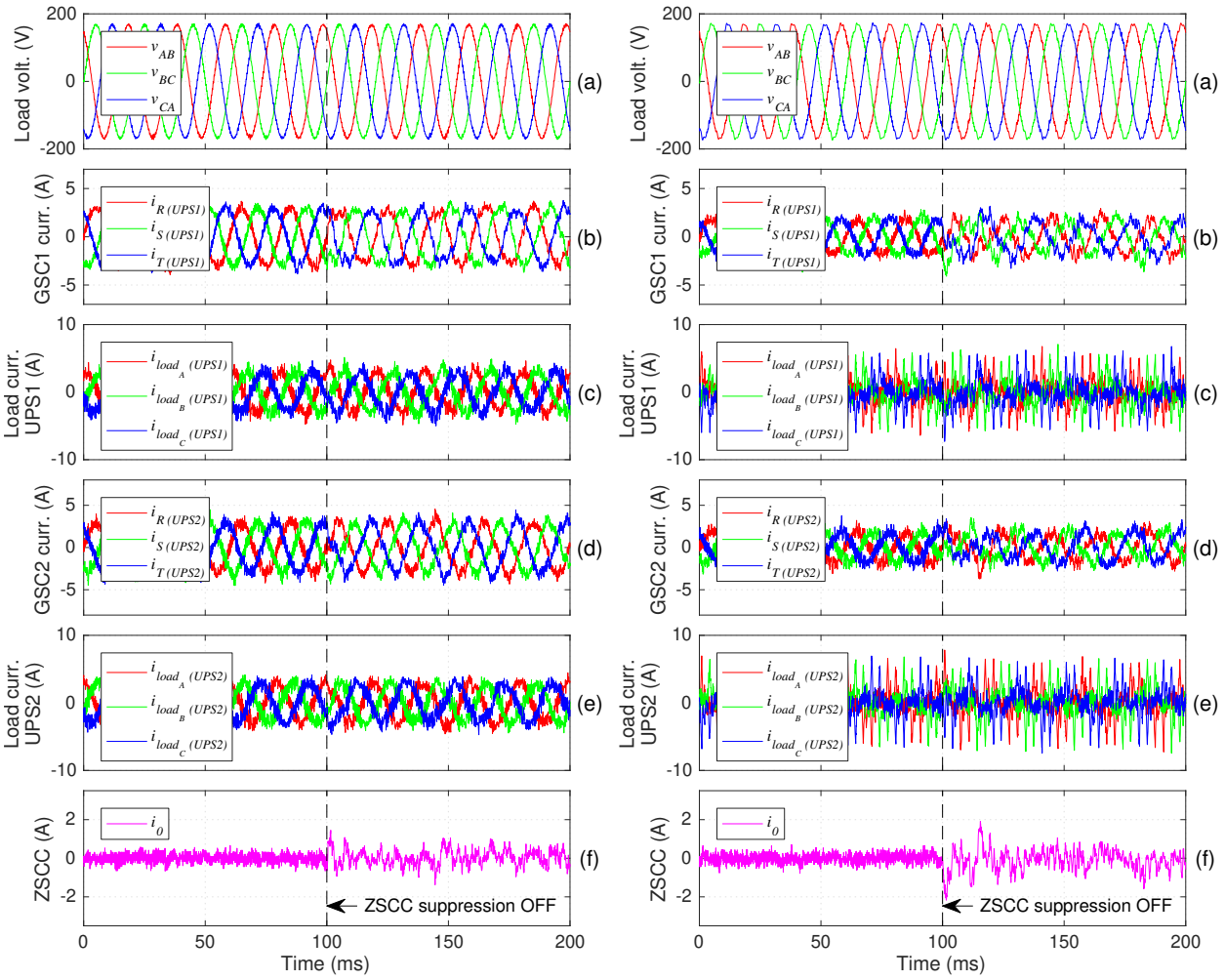
## 4.2 Parallel operation of the two UPS

The parallel operation of the system is now addressed. Firstly, the effectiveness of the control scheme in eliminating the ZSCC is demonstrated. Then, the load-sharing operation is presented. All the results were obtained for the two types of loads.

### 4.2.1 ZSCC suppression

Figure 4.7 shows the simulation results obtained when each UPS is supplying half of the load power ($\lambda_1 = 0.5$) to the linear load (Figure 4.7a) and to the non-linear load (Figure 4.7b). Until the instant marked with the dashed line, the ZSCC suppression is activated ($W_{z_G} = W_{z_L} = 1$). After that instant, the ZSCC suppression is deactivated ($W_{z_G} = W_{z_L} = 0$). After the ZSCC suppression deactivation, the ZSCC immediately reaches values of almost 2 A in both situations. Consequently, the harmonic distortion of the grid and load currents of

each UPS increases. In the non-linear load case, the magnitude of the ZSCC is very significant when compared to the phase currents absorbed/supplied by each UPS system, leading to highly distorted absorbed grid currents.

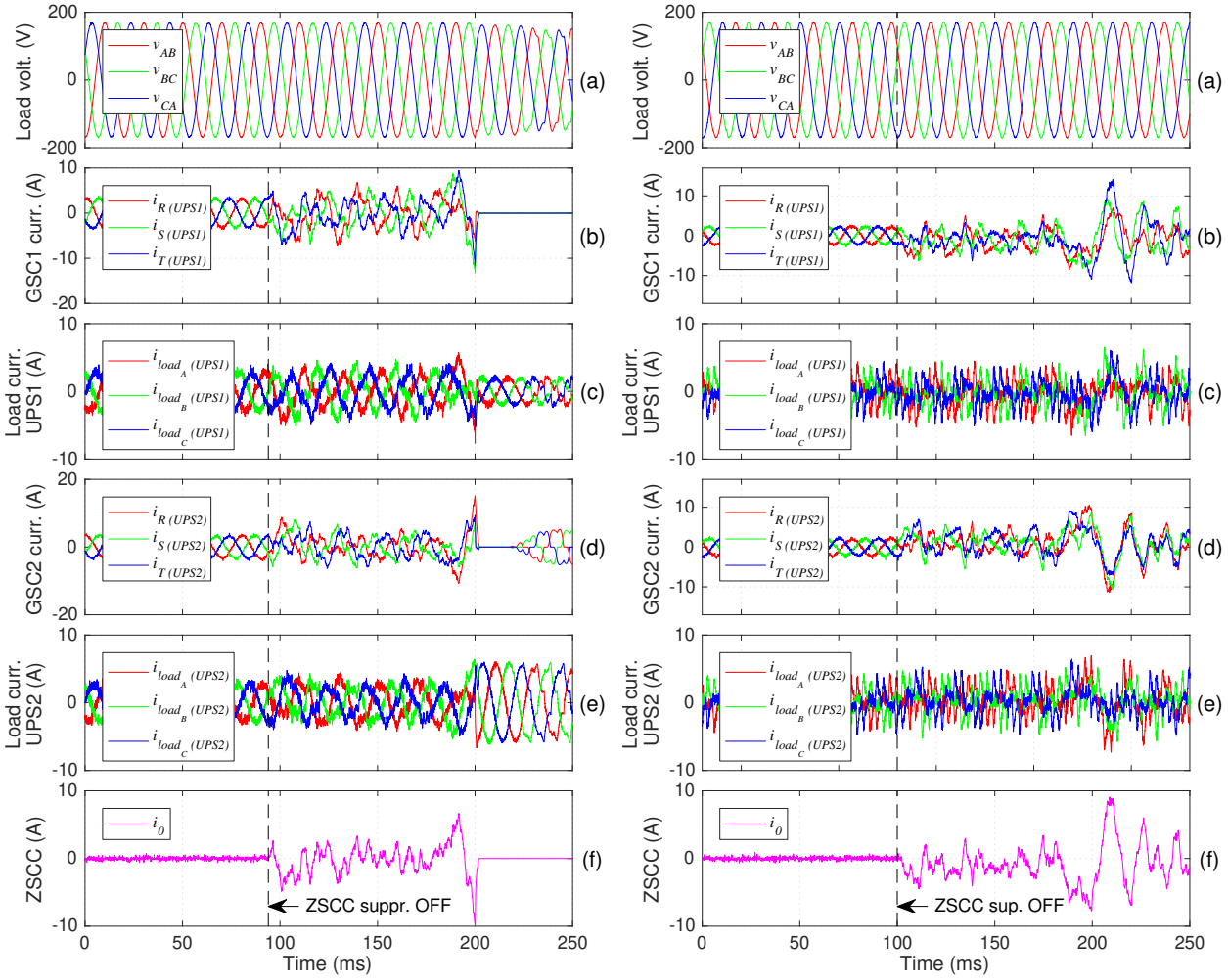



(a) Supplying the linear load.

(b) Supplying the non-linear load.

Figure 4.7: UPSs performance during the deactivation of the ZSCC suppression [Simulation].

Due to a high number of asymmetries in the experimental circuit (i.e. tolerance of the inductances and capacitors), the switching states patterns applied to both UPSs can severally differ over time. This can lead to switching states combinations between the converters that increase significantly the ZSCC. Therefore, the undesired effects of the ZSCC are typically much more visible in the experimental tests. This is demonstrated in Figure 4.8, for the two types of loads. For the same load-sharing conditions, after the instant marked with the dashed line the ZSCC suppression is deactivated and a considerable ZSCC immediately appears. Both for the linear and non-linear load, this current almost reaches 10 A leading to highly distorted currents in the systems. In the case of the test in which a linear load is used, the GSC2 current protection is actually activated, since the current of phase $R$ reaches 15 A (predefined maximum admissible current at each point of paralleled system).




(a) Supplying the linear load.

(b) Supplying the non-linear load.

Figure 4.8: UPSs performance during the deactivation of the ZSCC suppression [Experimental].

### 4.2.2 Asymmetric load-sharing operation

The response of the system during power distribution changes is demonstrated through simulation and experimental results, considering the linear load, in Figure 4.9 and Figure 4.10, respectively. Firstly, the UPS2 is providing all the load power (the IGBTs of the UPS1 are all switched OFF). Then, the coefficient $\lambda_1$ is sequentially incremented by 0.25 until the UPS1 system supplies the total load power.

When the percentage of the load power assigned to a UPS is set to zero, a load-side current is observed in the system. However, this current corresponds to an almost purely reactive current that circulates through the capacitors of the respective load-side filter. It can be seen from the output currents that the power supplied by each UPS changes immediately to the target value both in the simulation and experimental cases. A slower transition is observed in the displayed output average power simply because a time horizon of one period is considered in its calculation. It is possible to see that the ZSCC is effectively eliminated

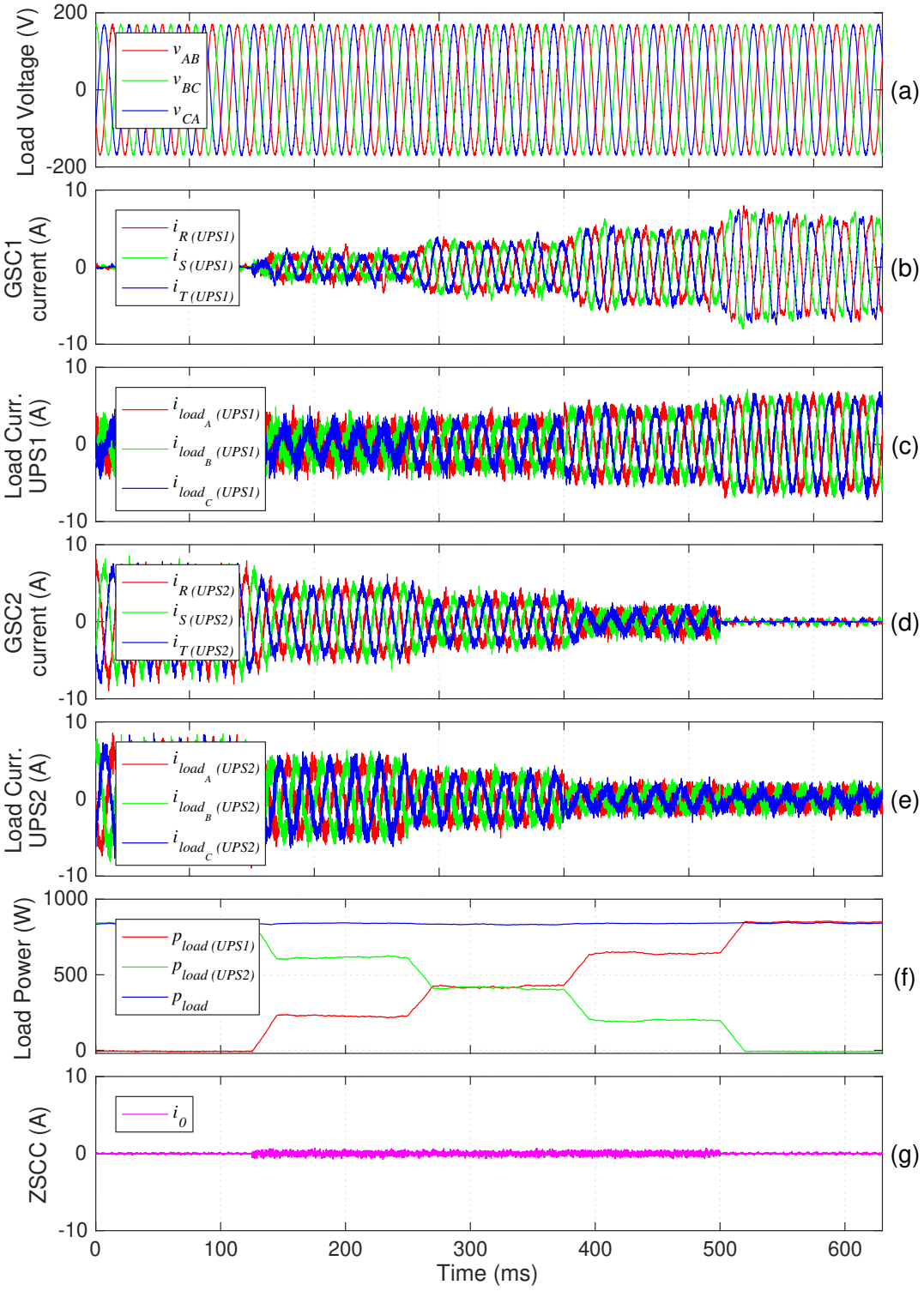



Figure 4.9: UPSs performance when different percentage of the power supplied to a linear load is assigned to each UPS [Simulation].

in any load-sharing condition. Therefore, it is possible to have stable and near sinusoidal currents in all the operation range of the two paralleled systems.

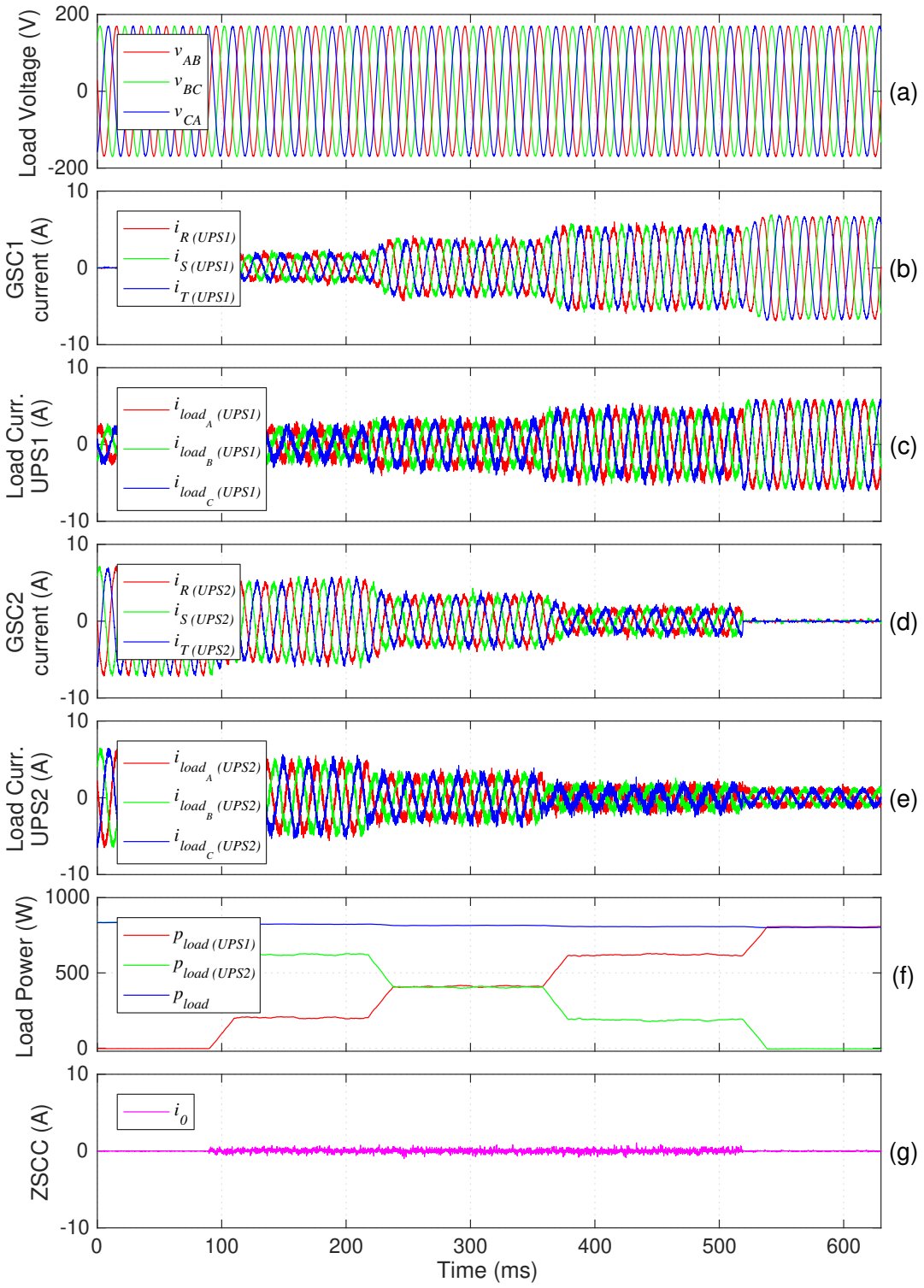



Figure 4.10: UPSs performance when different percentage of the power supplied to a linear load is assigned to each UPS [Experimental].

Figure 4.11 and Figure 4.12 demonstrate the effectiveness of the load-sharing control scheme when the UPS systems are feeding the non-linear load.

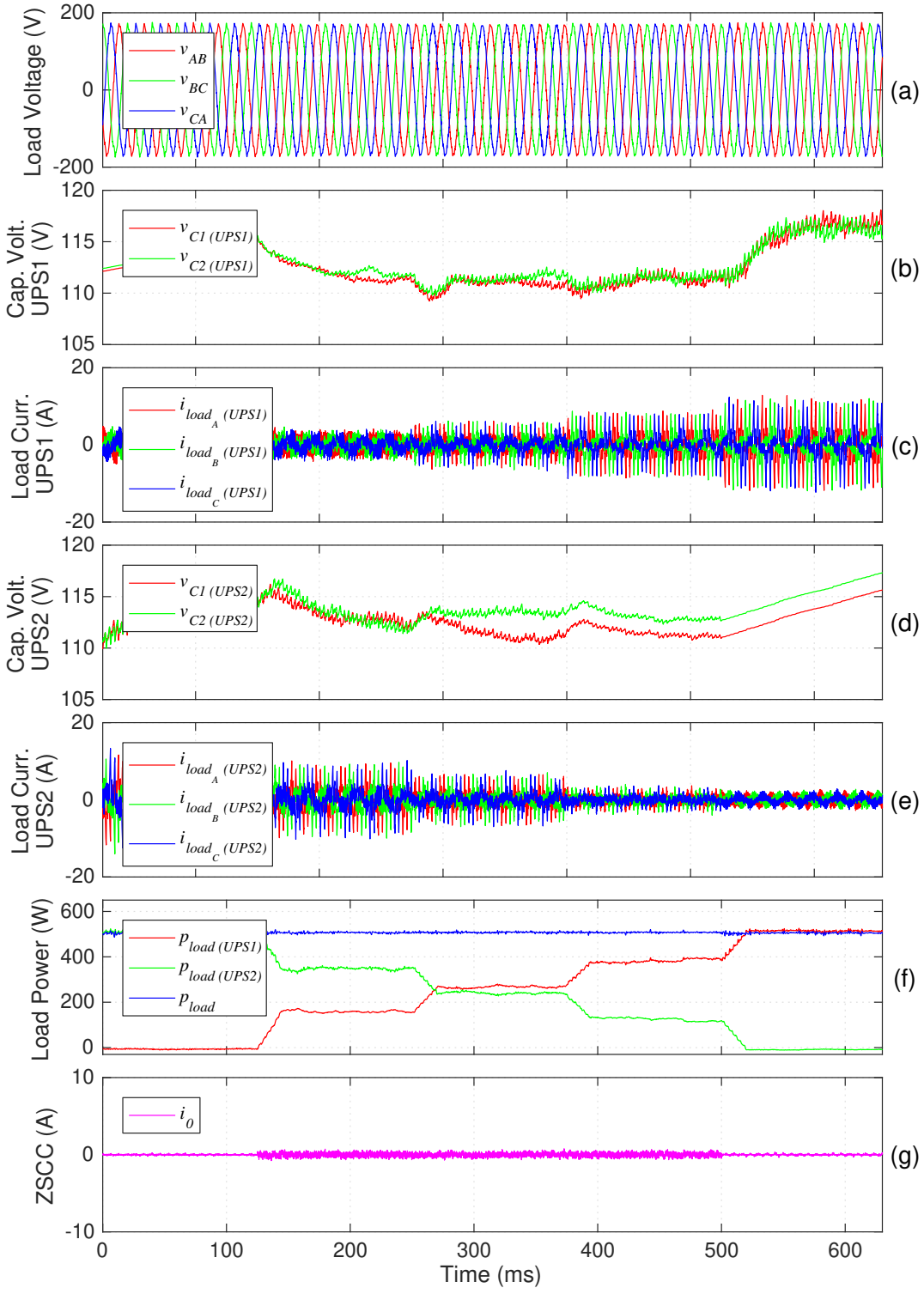



Figure 4.11: UPSs performance when different percentage of the power supplied to a non-linear load is assigned to each UPS [Simulation].

The systems were subjected to the same power variations of the previous case. As demonstrated in the simulation and experimental results, even when supplying a non-linear load, and simultaneously changing the load power distribution, high quality output voltage

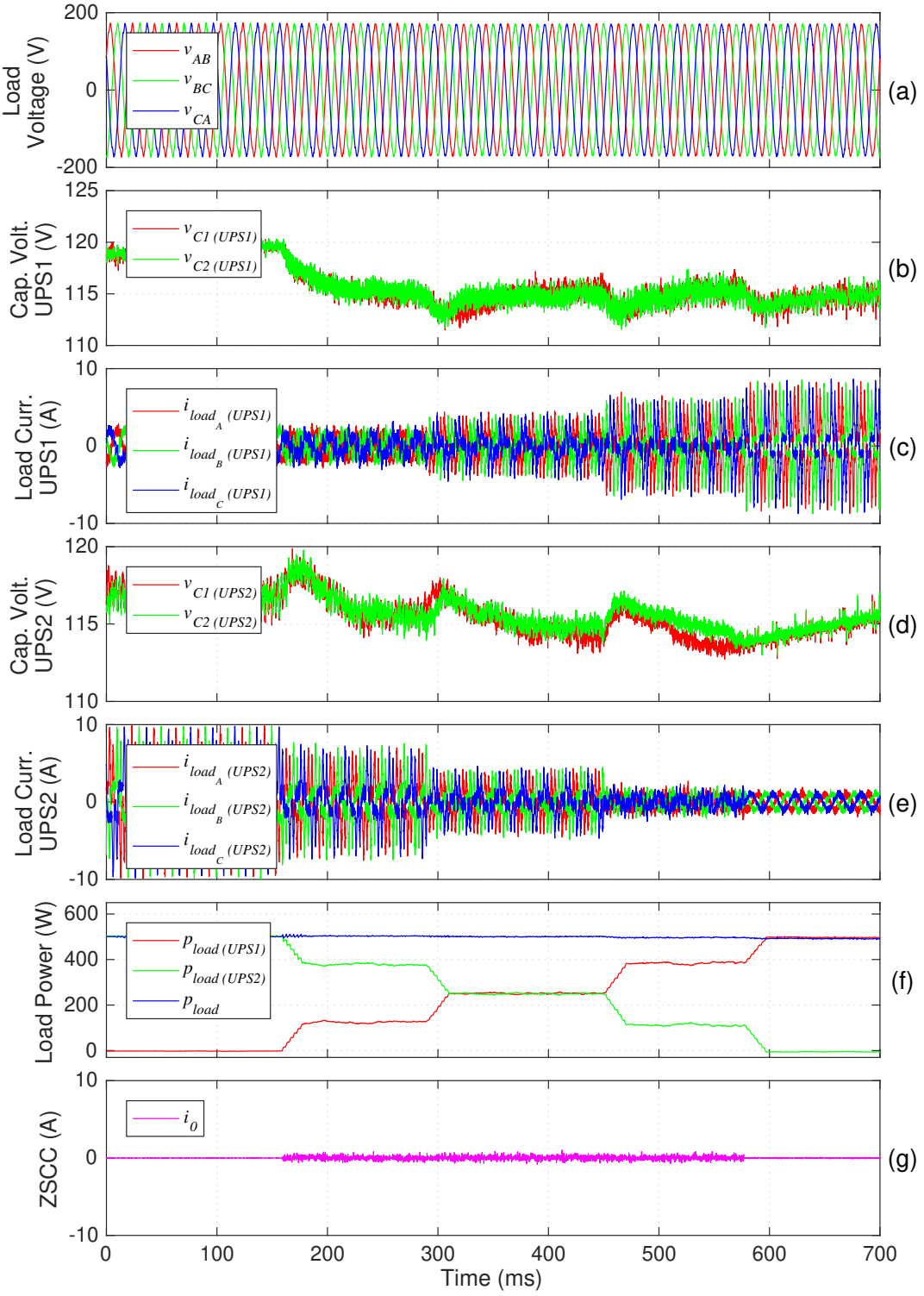



Figure 4.12: UPSs performance when different percentage of the power supplied to a non-linear load is assigned to each UPS [Experimental].

waveform is obtained. Moreover, during those fast distribution changes, the capacitors voltage balance is also ensured. When a UPS does not provide load to the power, an increase in DC bus voltage is observed. It happens because the input/outputs of both UPS are still

physically connected and the grid and load voltage are not synchronized, allowing that small currents can flow through the converters' diodes to the DC buses. However, this isn't a dangerous situation, since in the worst case (grid voltage in phase-opposition with the load voltage) the DC bus is subjected to a voltage of two times the peak of the grid/load voltage (in this case $2\sqrt{2} \times 120 \approx 338V$). This situation can be undesirable when the UPSs are working with higher voltages. In this case, it is recommended to generate the load voltage reference considering the phase of the grid voltage given by the PLL.

Figure 4.13 and Figure 4.14 represent the measures taken with the respective UPS power analyzers when each UPS system is providing 50 % of the load power.

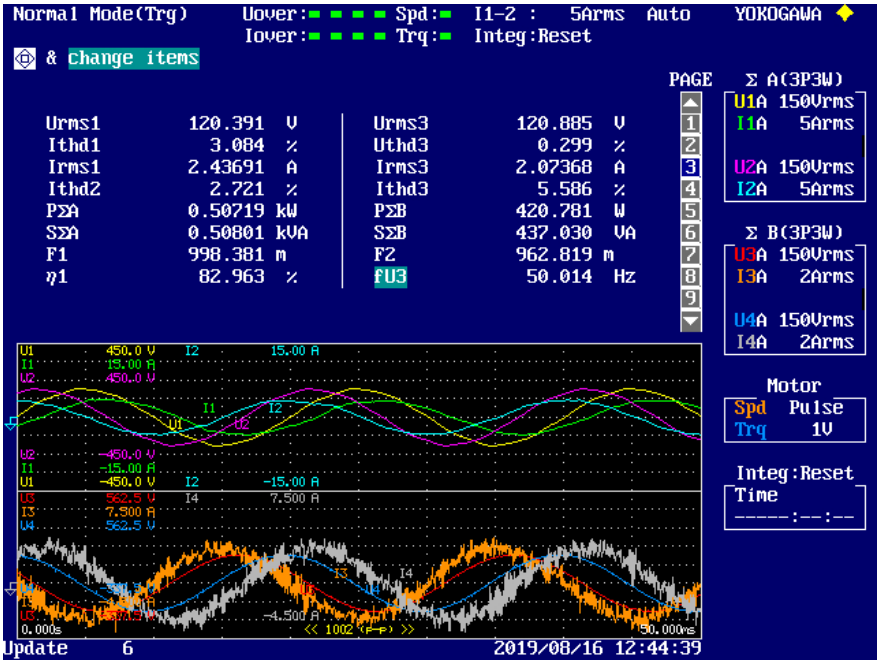



Figure 4.13: Power analyzer results (UPS1) when the linear load is equally shared by the two systems ($\lambda_1 = 0.5$).

Two grid-side and two load-side voltage and current waveforms are provided by the respective analyzer. Accordingly to the power analyzers, the UPS1 is absorbing approximately 507 W (P$\sum$A), whereas UPS2 is absorbing about 491W[3]. Both UPS are absorbing power with approximately unit power factor (F1 $\approx$ 0.998 in both systems). Each system is providing approximately 421 W and 405 W to the load ($P \sum B$). Thus, an efficiency of about 82 % ($\eta_1$) is obtained in both systems. The grid-side and load currents present low harmonic distortion: 3.084 %/3.401 % and 5.586 %/4.668 % for UPS1/UPS2 grid and load currents, respectively. The observed ripple in the UPSs load currents is caused by the remaining ZSCC that cannot be eliminated by the control scheme (due to the communication constrains between UPS controllers during a control sampling time). This ripple does not appear in the grid currents just because for the grid-side measurements, a low-pass line filter (internal to the power

[3]Due to the aperiodic behaviour of FCS-MPC, some variation in the results provided by the power analyzer was observed.

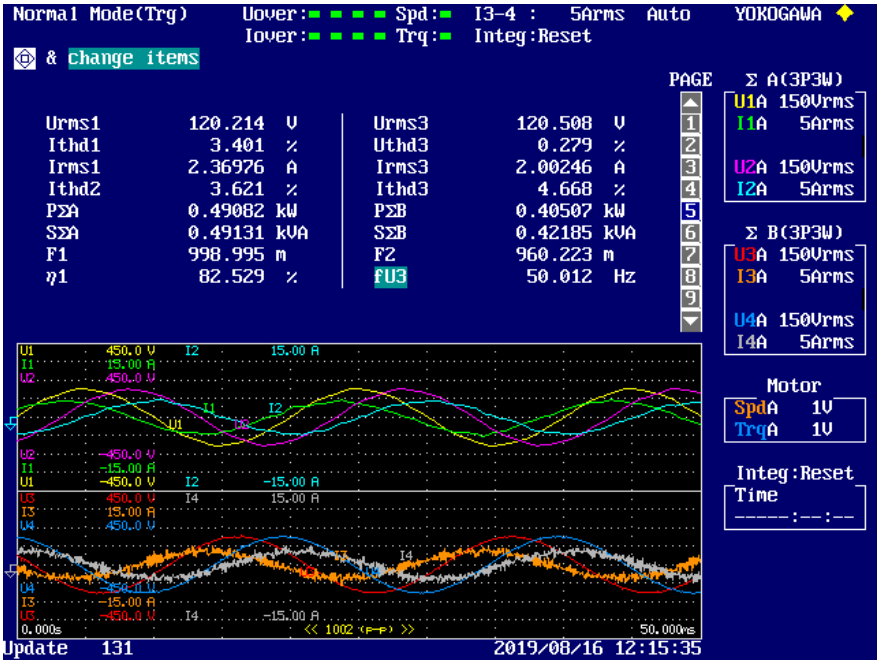
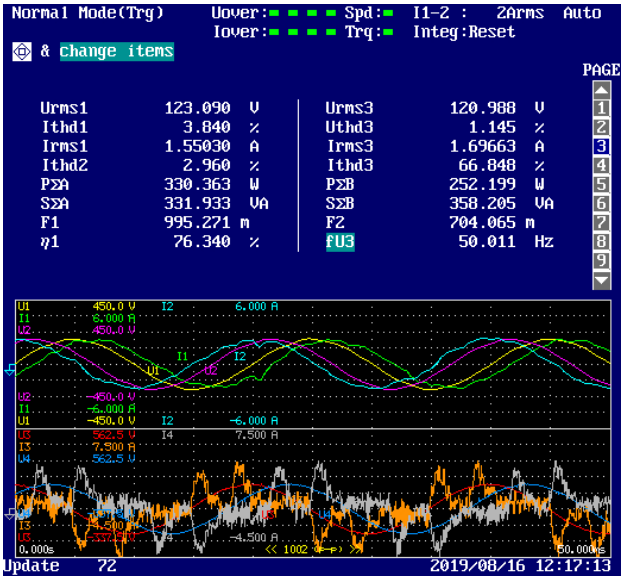



Figure 4.14: Power analyzer results (UPS2) when the linear load is equally shared by the two systems ($\lambda_1 = 0.5$).

analyzer, cutoff frequency = 500Hz) was considered to effectively visualize the currents being absorbed by each UPS and provide stable PLL response and measurements. Regarding the generated load voltage, both the power analyzers indicate a RMS value of approximately 120 V and a THD of about 0.3%. These are very good results, since the output voltage is being generated in conjunction by the two UPSs in which the load voltage is not directly controlled.

In Figure 4.15, are presented the power analyzer results that demonstrate the performance of the system when the non-linear load is equally shared by the two UPS systems ($\lambda_1 = 0.5$). In this situation the active power supplied by the UPS1 and UPS2 is respectively 252 W and 239 W. Compared to the previous case, lower efficiency is observed in both systems ($\approx$ 76 %). This happens because the power losses in the passive components (filters, wires and DC capacitors) as well as the switching losses present a more significant value in comparison to the power supplied by the systems to the load. It is possible to conclude that even when feeding a non-linear load, an high-quality voltage waveform is also generated (with THD of $\approx$ 1.2 %).

The detailed measurements that demonstrate the performance of the UPS systems during asymmetric power distribution are shown in Figure 4.16. In Figure 4.16a the UPS1 is supplying 75 % of the load power, whereas in Figure 4.16b the UPS2 is providing the remaining 25 % of the power to the load. It is possible to see that even during the asymmetric sharing of a non-linear load current, a high-quality load voltage waveform is obtained. In the presented load-sharing condition, both UPS systems are absorbing power with practically unit power factor.




(a) UPS1 providing 50 % of the load power.


(b) UPS2 providing 50 % of the load power.

Figure 4.15: Power analyzer results when the systems are equally sharing a non-linear load.


(a) UPS1 providing 75 % of the load power.


(b) UPS2 providing 25 % of the load power.

Figure 4.16: Power analyzer (UPS2) results during asymmetrically non-linear load sharing.

In Table 4.3 and Table 4.4 are presented the powers absorbed and supplied by each UPS during different load sharing conditions regarding the linear and non-linear load, respectively. All the powers were obtained through the power analyzers of both UPSs. The efficiency of each UPS ($\eta_1$ and $\eta_2$) and the overall efficiency ($\eta_{Total}$) of the system are also presented. It can be observed in both tables that the efficiency of a UPS increases with the load. Moreover, a similar behaviour can be observed regarding the overall system efficiency: the higher efficiency values are obtained when each UPS is providing 100 % of the load power. In this case the IGBTs of the UPS that isn't providing power to the load are all OFF and the respective

switching losses are null. During the other tested load-sharing conditions, higher overall efficiency is obtained for a 50 %/50 % distribution. These efficiency values suggest that when the power absorbed by the load is bellow the power ratings of a UPS, a 0/100 % distribution leads to the highest overall efficiency, and in this case the stress imposed to the paralleled UPSs can be managed. When the power absorbed by the load exceeds the ratings of a UPS, it has to be distributed between the two paralleled systems. In this case, there might be several load-sharing conditions that lead to high overall system efficiency.

Table 4.3: Powers (W) and efficiencies (%) when the linear load is supplied.

| $\lambda_1$ | $\lambda_2$ | $P_{grid_{(1)}}$ | $P_{load_{(1)}}$ | $\eta_1$ | $P_{grid_{(2)}}$ | $P_{load_{(2)}}$ | $\eta_2$ | $P_{grid_{Total}}$ | $P_{load_{Total}}$ | $\eta_{Total}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | - | - | - | 998.03 | 840.59 | 84.22 | 999.67 | 840.59 | 84.09 |
| 0.25 | 0.75 | 260.44 | 201.83 | 77.50 | 749.74 | 623.76 | 83.20 | 1010.18 | 825.59 | 81.73 |
| 0.5 | 0.5 | 507.19 | 420.78 | 82.96 | 490.82 | 405.07 | 82.53 | 998.01 | 825.85 | 82.75 |
| 0.75 | 0.25 | 767.02 | 638.42 | 83.23 | 232.96 | 180.48 | 77.47 | 999.98 | 818.90 | 81.89 |
| 1 | 0 | 983.49 | 822.33 | 83.61 | - | - | - | 984.62 | 822.33 | 83.52 |

Table 4.4: Powers (W) and efficiencies (%) when the non-linear load is supplied.

| $\lambda_1$ | $\lambda_2$ | $P_{grid_{(1)}}$ | $P_{load_{(1)}}$ | $\eta_1$ | $P_{grid_{(2)}}$ | $P_{load_{(2)}}$ | $\eta_2$ | $P_{grid_{Total}}$ | $P_{load_{Total}}$ | $\eta_{Total}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | - | - | - | 617.00 | 494.93 | 80.22 | 618.54 | 494.93 | 80.02 |
| 0.25 | 0.75 | 189.80 | 123.98 | 65.32 | 471.30 | 366.45 | 77.75 | 661.10 | 490.43 | 74.18 |
| 0.5 | 0.5 | 330.36 | 252.20 | 76.34 | 311.25 | 238.75 | 76.71 | 641.61 | 490.95 | 76.52 |
| 0.75 | 0.25 | 488.62 | 382.57 | 78.30 | 163.78 | 112.38 | 68.62 | 652.40 | 494.95 | 75.87 |
| 1 | 0 | 612.39 | 492.00 | 80.34 | - | - | - | 613.59 | 492.00 | 80.18 |

# Chapter 5

# Conclusions and Future Work

## 5.1 Conclusions

In this dissertation a control scheme for controlling two paralleled uninterruptible power supply systems (UPS) was proposed.

Firstly, a review on relevant topics to the work was made, including the UPS types and available control strategies for power electronics converters. Among the available types of uninterruptible power supplies (UPS) a paralleled system based on two double conversion UPS was adopted. Regarding the control type, due to its intuitive concept, fast transient response, and flexibility to operate in a multi-converter system, Finite Control Set Model Predictive Control (FCS-MPC) was selected to control all the converters.

The mathematical model of the system was presented and the dynamics of the zero sequence circulating current (ZSCC) was demonstrated in detail. A description of the control strategies adopted in all the converters was also presented.

The proposed control scheme was tested in *Matlab/Simulink* environment and implemented in a real digital controller. Due to experimental limitations, different filters were used in the two systems.

The simulation and experimental results demonstrated that with the developed algorithm both UPS systems present high performance operation. With the proposed controller, the two paralleled systems provide very fast response to the variations in the load power distribution for the two types of load. It was also demonstrated that for any type of load and load-sharing conditions, the circulating current is effectively suppressed and a precise load-sharing obtained, with an high-quality voltage waveform being generated.

## 5.2 Suggestions for future work

Based on the developed work and achieved results presented in this dissertation, suggestions for future research can be given:

- Implement the developed control scheme in two independent controllers;
- Implement the control strategy in a higher power system;
- Consider a neutral point in each UPS system to provide 4-wire capabilities such as the connection of multiple single-phase loads;
- Develop a power management algorithm that automatically distributes the load power between the UPSs to optimize the overall efficiency of the system and to manage the stress of the paralleled systems.

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# Appendix A

# Simulation Model Details

This appendix gives an overview about the developed simulation model. The main electrical and control parameters considered in the simulation are also described.

## A.1 Simulation Model Overview

In the Figure A.1 is represented a global view of the developed simulation model implemented in *Matlab/Simulink*. As the figure shows, all the electrical elements were considering including the power grid, the 4 power converts, the DC buses, the filters and the critical load. The control blocks are implemented in the subsystems inside the yellow-shaded area. The weighting factors and power distribution can also be regulated when the simulation is running by changing the constants of the purple- and red-shaded areas, respectively.

In Figure A.2 the main control steps regarding GSC1 are represented. The green-shaded are correspond the grid current references calculation, which can be seen with more detail in Figure A.4. The variables prediction at $k+1$ and objective function minimization blocks are made in the functions represented by the red and blue areas, respectively. Similarly, Figure A.3 illustrates the control implemented in LSC1. The load-side currents reference calculation, variables prediction at $k+1$ and objective function minimization are represented in the green, red and blue areas.

## A.2 Simulation Parameters

The main parameters adopted in the simulation model are represented in the Tables A.1, A.2, A.3 and A.4.

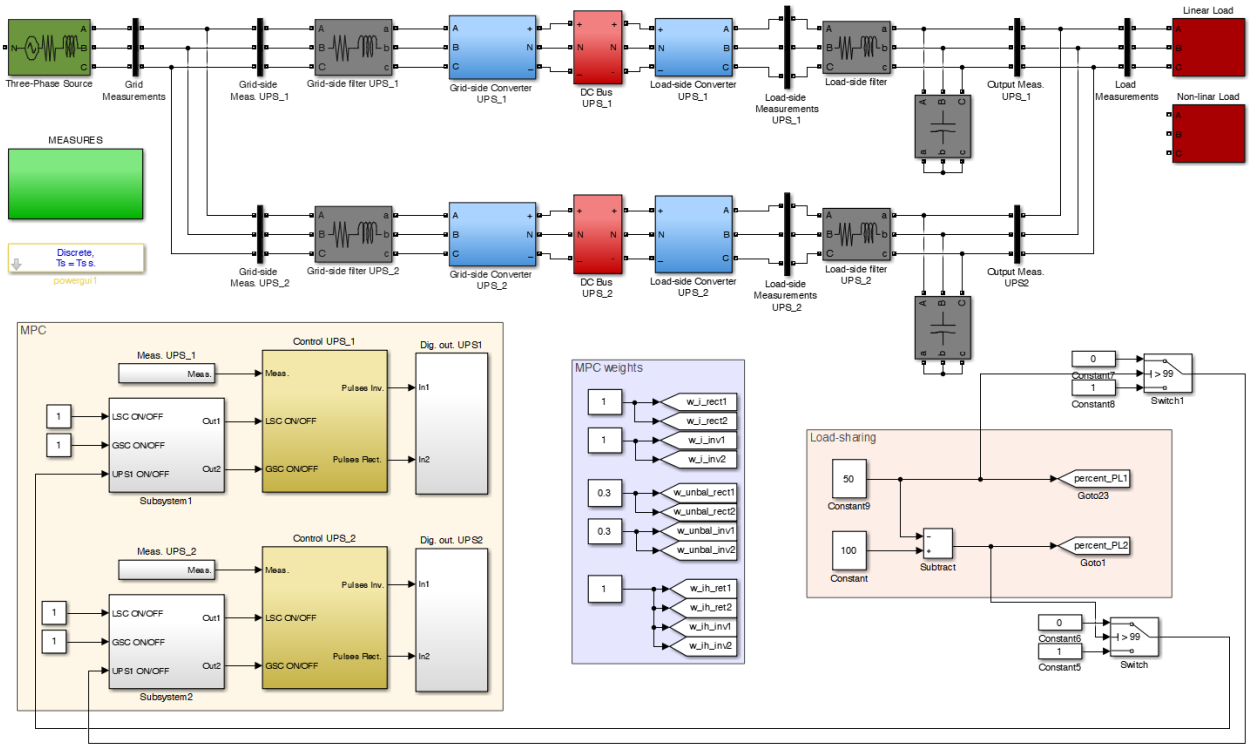



Figure A.1: Overview of the simulation model implemented in *Matlab/Simulink*.

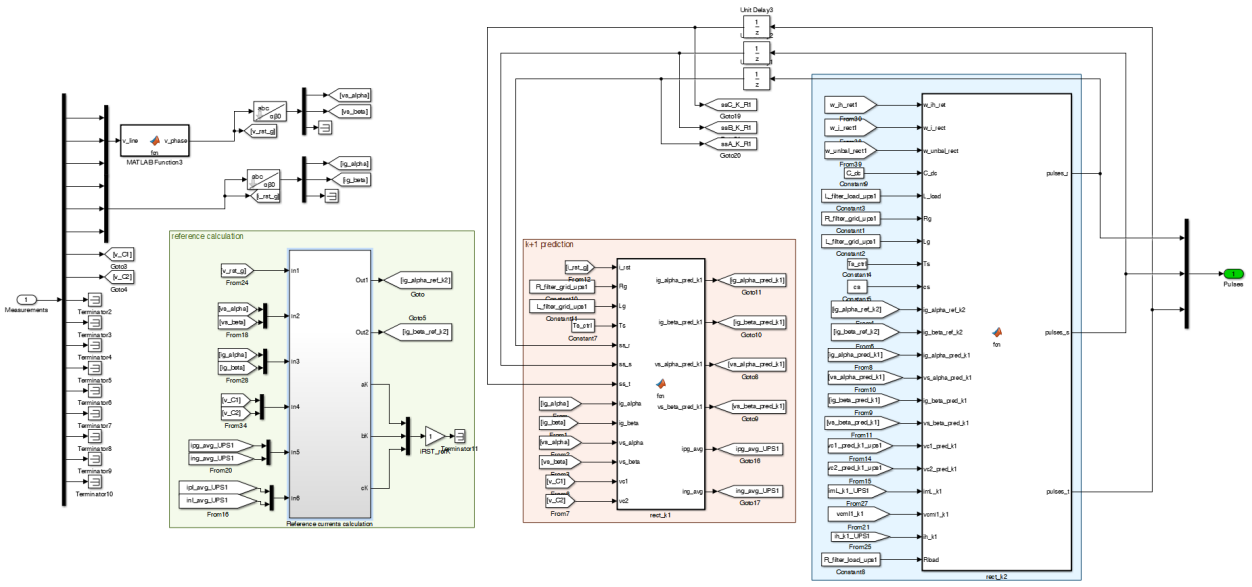



Figure A.2: Overview of the GSC1 control implemented in *Matlab/Simulink*.

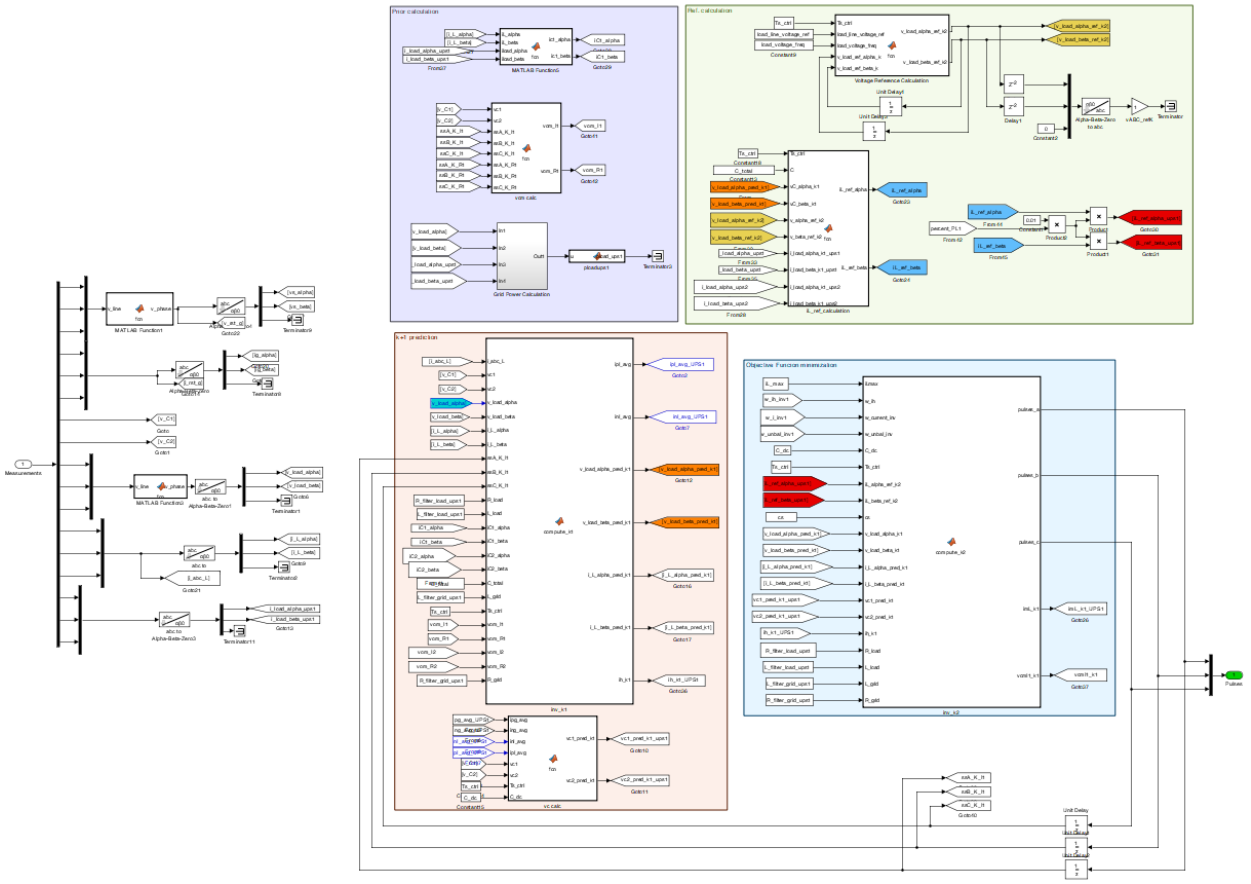


Figure A.3: Overview of the LSC1 control implemented in *Matlab/Simulink*.

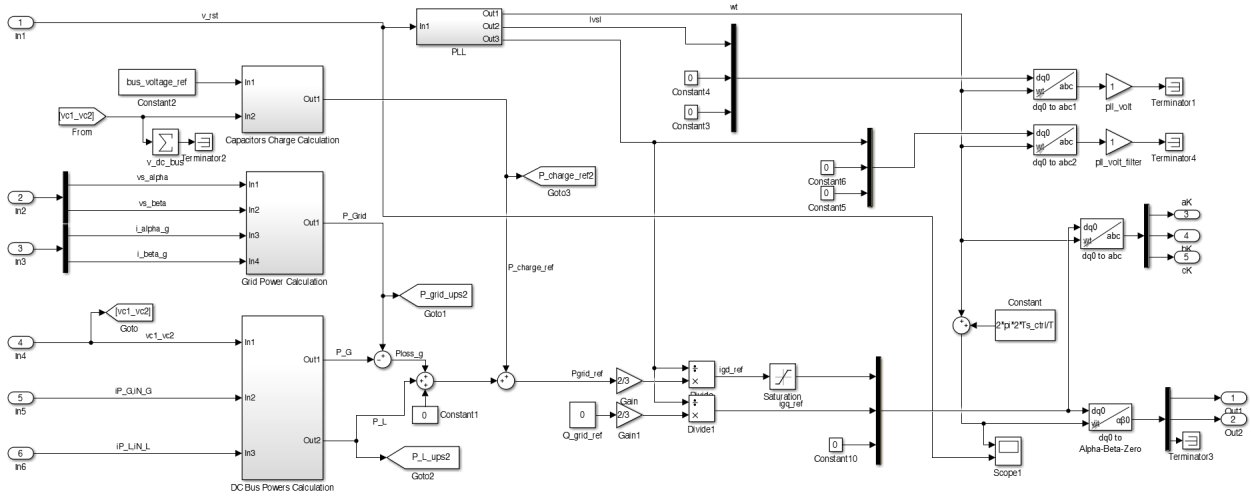



Figure A.4: Overview of the grid current references calculation for the GSC1 implemented in *Matlab/Simulink*.

Table A.1: Electrical parameters of the simulation model.

| Parameter | Value |
|---|---|
| Grid line voltage (RMS) | 120 V |
| Grid voltage frequency | 50 Hz |
| UPS1 grid-side filter | 13.5 mH |
| UPS2 grid-side filter | 5 mH |
| UPS1 and UPS2 DC bus capacit. | 3 mF |
| LSC1 and LSC2 filter inductance | 2.7 mH |
| LSC1 load-side filter capacitance | 66 $\mu$F |
| LSC2 load-side filter capacitance | 33 $\mu$F |

Table A.2: Simulation semiconductor parameters.

| Parameter | Value |
|---|---|
| IGBT and Diode ON resistance | 1 m$\Omega$ |
| IGBT and Diode ON inductance | 0 |
| IGBT forward voltage | 1.45 V |
| Diode forward voltage | 1.4 V |
| Diode and IGBT snubber resistance | 100 k$\Omega$ |
| IGBT snubber capacitance | 0.22 $\mu$F |

Table A.3: Simulation control parameters.

| Control Parameter | Value |
|---|---|
| Load line voltage (RMS) | 120 V |
| Load voltage frequency | 50 Hz |
| DC charge horizon ($N_{th}$) | 500 |
| UPS1 and UPS2 DC bus voltage reference | 220 V |

Table A.4: Simulation Sample Times.

| Simulation Parameter | Value |
|---|---|
| Electrical sample time | 1 $\mu$s |
| Control sample time ($T_s$) | 70 $\mu$s |

# Appendix B

# Experimental Setup Details

In this Appendix are presented the main components of the experimental setup. The full experimental setup is represented in Figure B.1 and B.2.

## B.1 UPS1 System

Figure B.3 shows the LSC1 prototype. A more detailed illustration of this prototype is in Figure B.4. As this Figure shows, this prototype has two sensor boards. Each board contains 3 current sensors and 3 voltage sensors. The voltage signals at the output of these boards are within the range [-10, 10 V]. The current and voltage sensors have gain of 3 and 65 respective (similar sensor boards were used in the rest of the system). This converter uses *Semikron* power modules that have a rated current of 20 A and a rated voltage of 600 V (per semiconductor). Each power module includes a *Semitop SK20MLI066* full NPC converter leg (Figure B.5 and B.6a). The IGBTs are driven using *Semikron Skyper 32PRO R* drivers (Fig.B.6b)

The GSC1 prototype is shown in Figure B.7. This prototype receives all the UPS1 IGBTs activation signals. All the required signal condition for the UPS1 is made inside this prototype including optical isolation and deadtime generation between complementary IGBT pulses (to avoid short-circuits). In this prototype, instead of a full NPC converter leg, half-bridge *SEMiX 202GB066HDs* IGBT power modules are used with rated voltage of 600 V and current of 200 A (Figure B.8). The IGBTs drivers used in this prototype are the same of the LSC1 prototype (*Semikron Skyper 32PRO R*).

The grid-side and load-side filters used in the UPS1 system are shown in Figure B.9.

## B.2 UPS2 System

In Figure B.10 are represented the two converters regarding UPS2. Fixed to each heat sinker is a H20R1203 IGBT and a VS-40EPF12 clamping diode (Figure B.11). The IGBTs are also driven by the *SKYPER 32PRO R* drivers (Figure B.12). Protection is provided to the

*dSpace controller* using the isolation board represented in Figure B.13. The activation pulses send by the controller are routed to the drivers using the pulse directing boards represented in Figure B.14 and B.15.

The grid-side and load-side filters used in UPS2 system, are represented in Figure B.16

## B.3 Used Digital Controller

During the realization of the experimental tests, a *dSpace MicroLabBox* was used (Figure B.17). The platform contains a dual-core PPC microprocessor which was programmed in *Matlab/Simulink* using the developed simulation model with blocks from the *dSpace RTI* and *RTI-MP* toolboxes. The control algorithm of each UPS was mainly implemented in each core. Using the *dSpace ControlDesk Next Generation* a control panel to control and monitor the paralleled systems was developed. Using this software it is also possible to acquire data to an external file, at sampling frequency and change the main control references in real time. All the relevant waveforms are displayed in the control panel, as displayed in Figure B.18.

## B.4 Other Components

The autotransformer and the critical loads are depicted in Figure B.19 and Figure B.20 respectively.

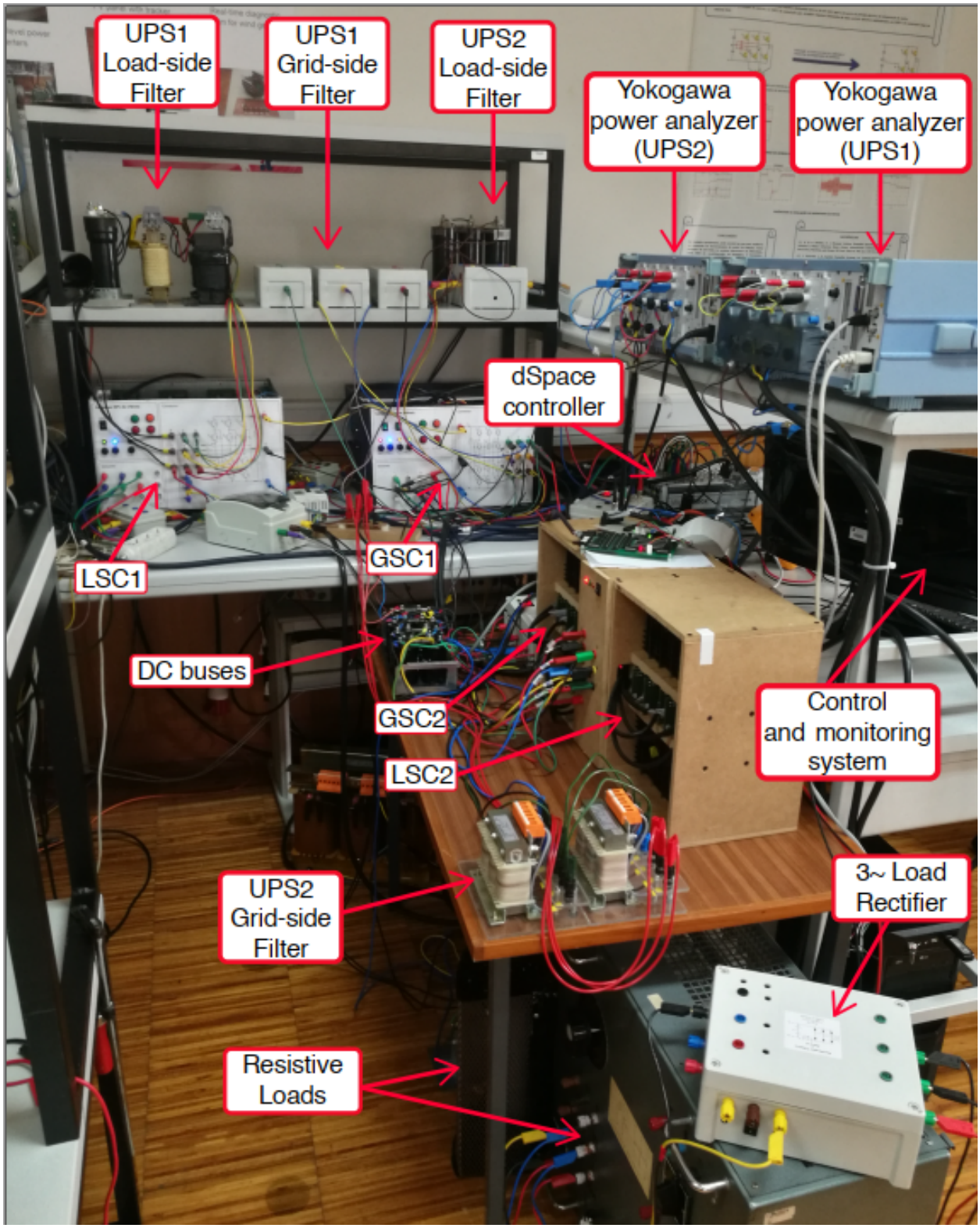



Figure B.1: Global view of the experimental setup.

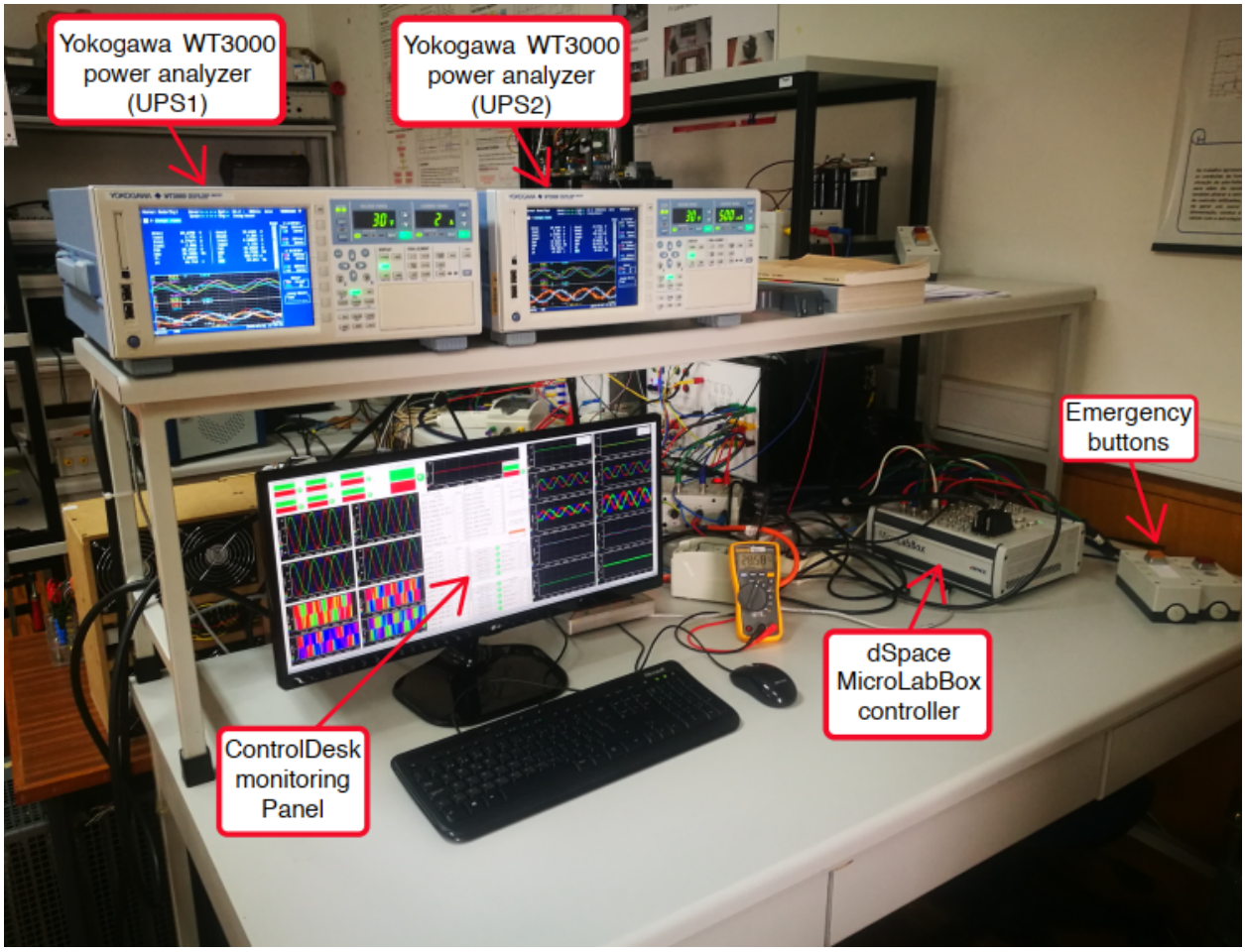



Figure B.2: Global view of the experimental setup and control system.

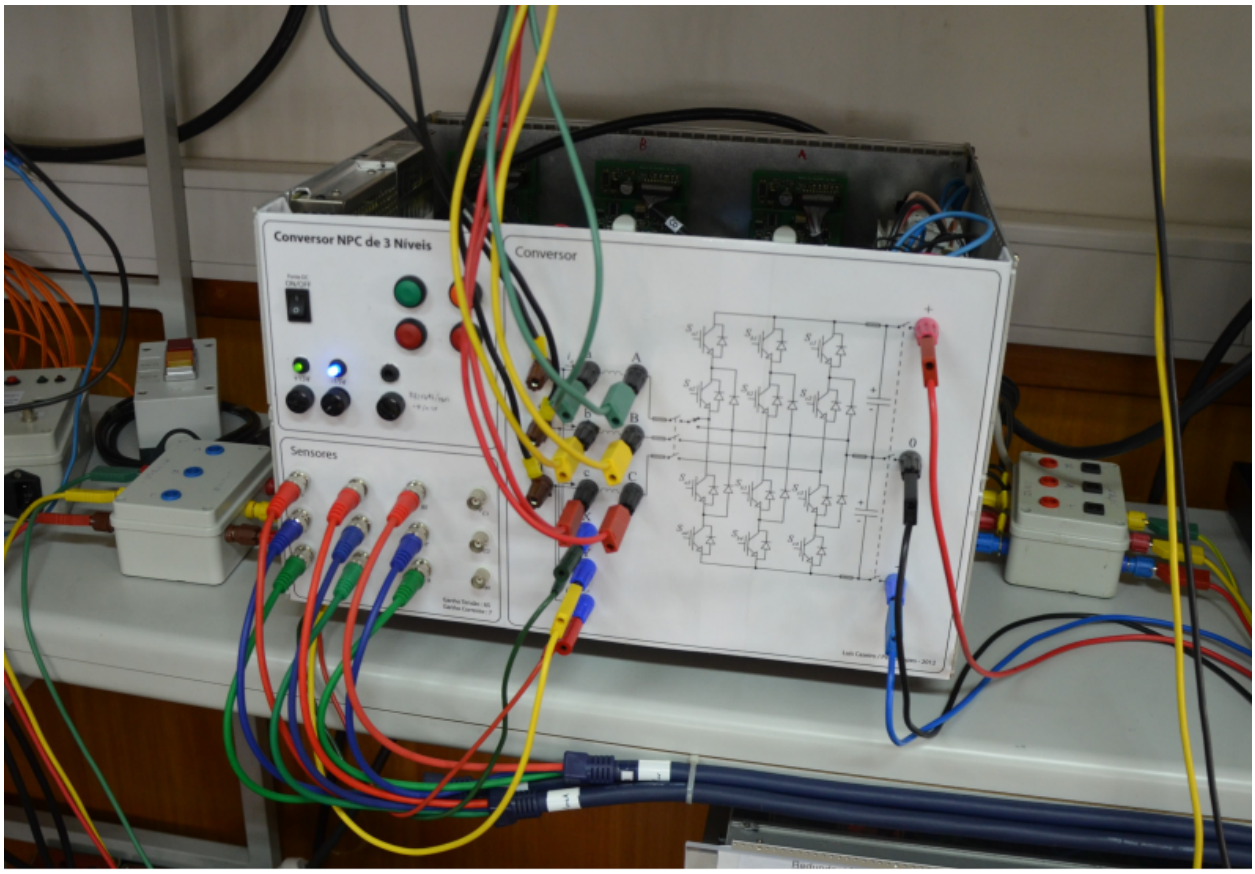



Figure B.3: Global view of the LSC1 prototype [2].

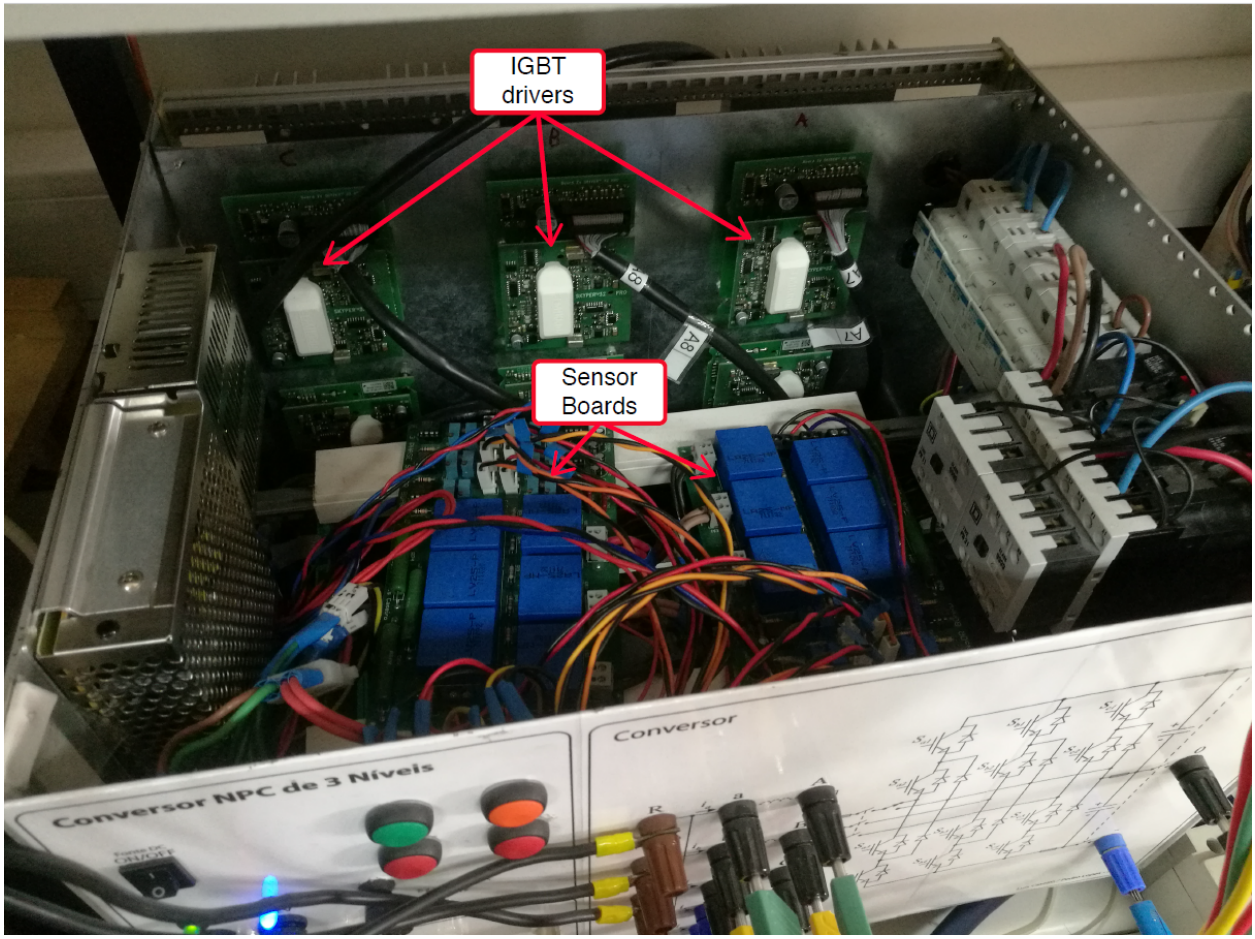



Figure B.4: Partial view of the LSC1 prototype.

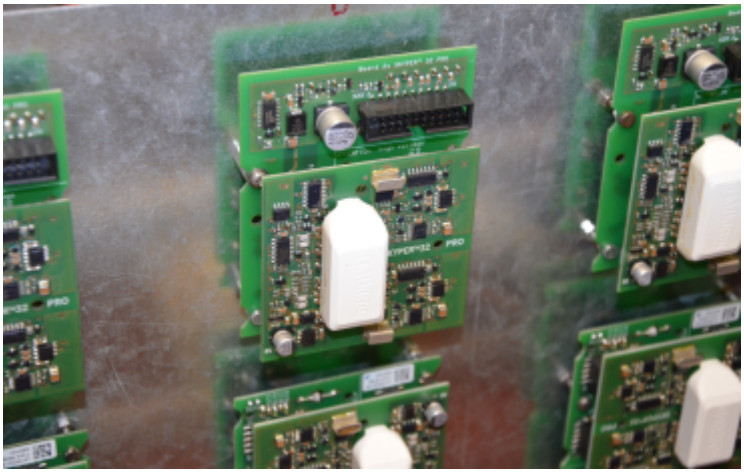
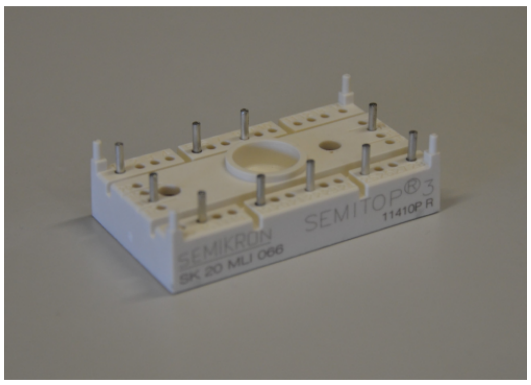
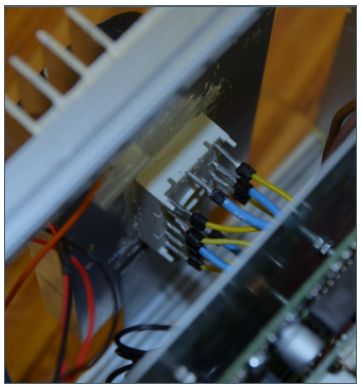


Figure B.5: IGBTs drivers in the LSC1 [2].




(a) Full NPC converter leg.



(b) Leg-Driver connection.

Figure B.6: Full NPC converter leg and driver connection (LSC1) [2].

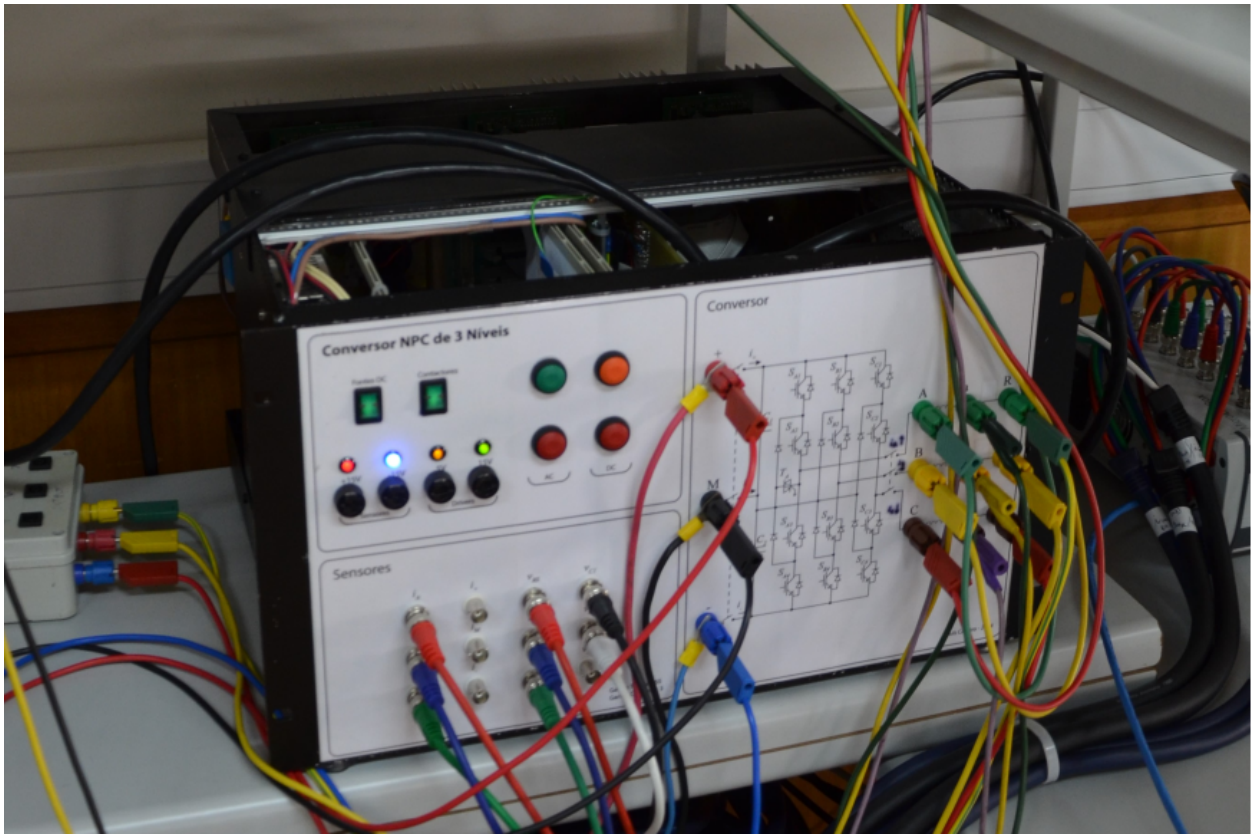



Figure B.7: GSC1 prototype [2].

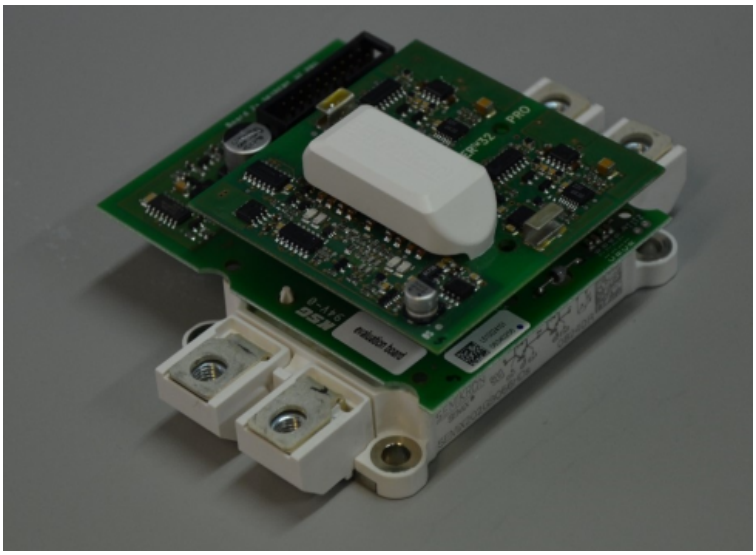


Figure B.8: Half-bridge power modules used in the GSC1 prototype [2].

(a) UPS1 load-side filter.

(b) UPS1 grid-side filter.

Figure B.9: Filters used in UPS1.

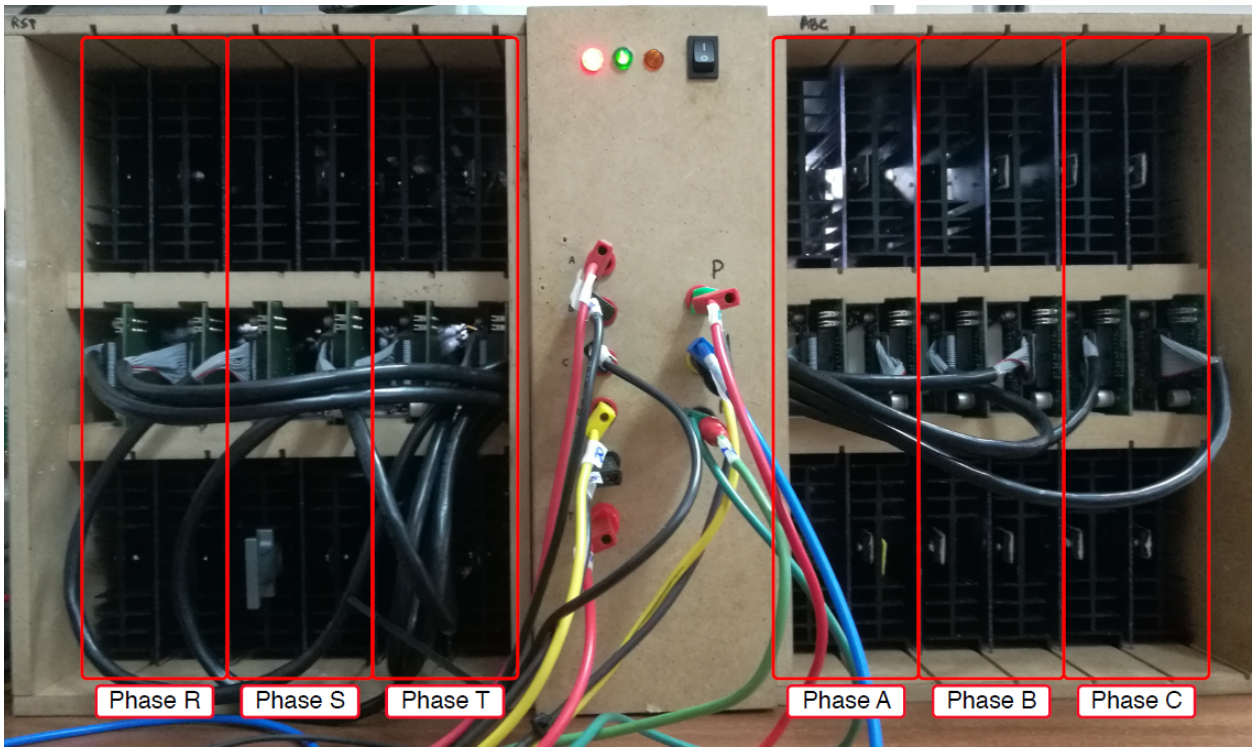



Figure B.10: UPS2 converters.

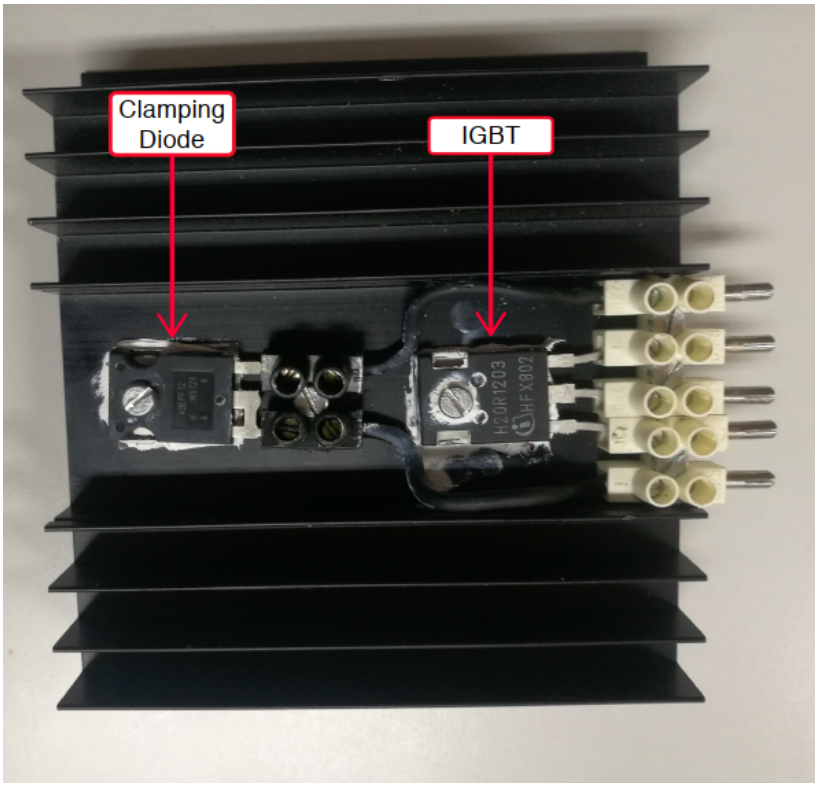



Figure B.11: IGBT and clamping diode (UPS2).

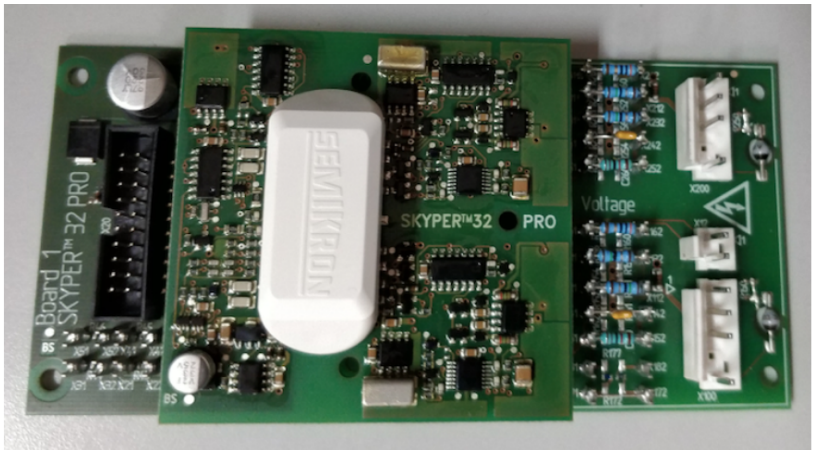



Figure B.12: IGBTs drivers used in UPS2.

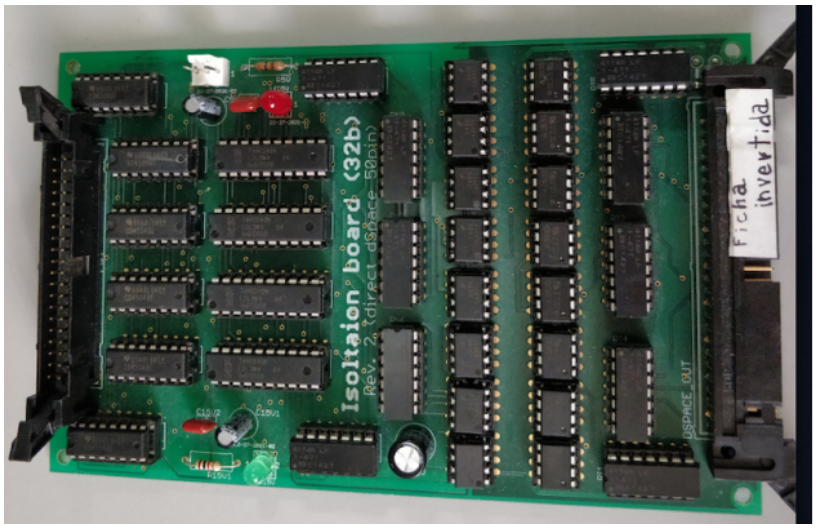



Figure B.13: Isolation board used in UPS2 system.


Figure B.14: Pulse directing board (UPS2).

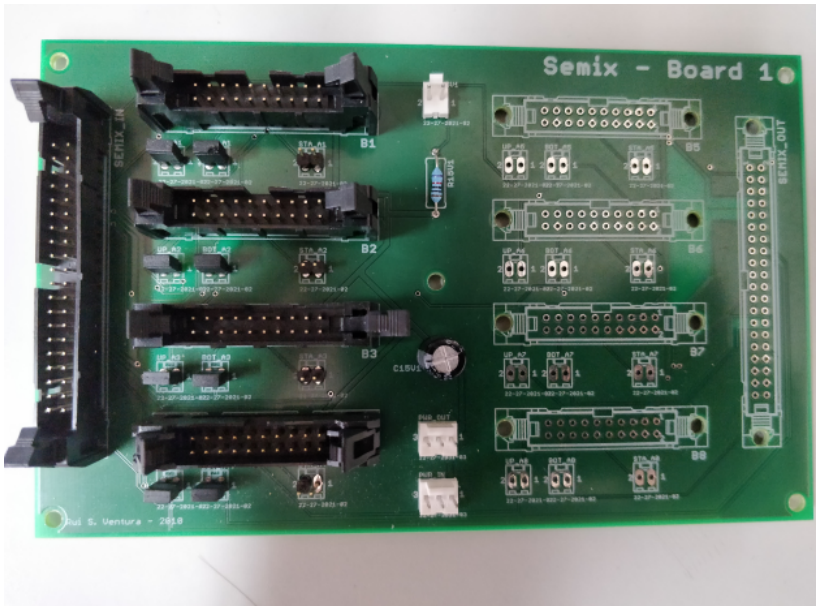
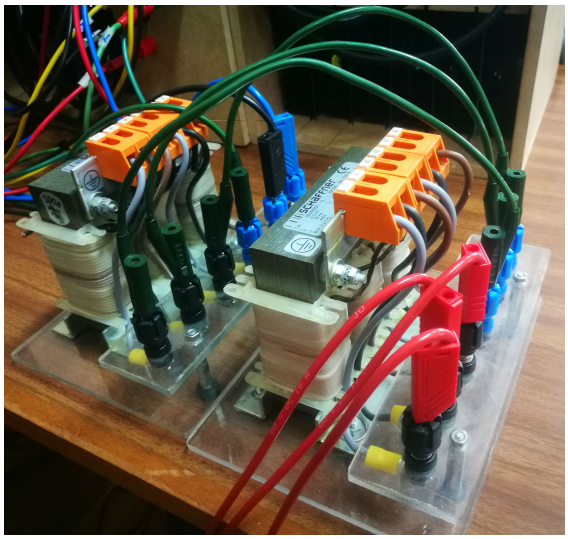



Figure B.15: Pulse directing board (UPS2).

(a) UPS2 load-side filter.



(b) UPS2 grid-side filter.

Figure B.16: Filters used in UPS2.


Figure B.17: Used *dSpace MicroLabBox* controller.

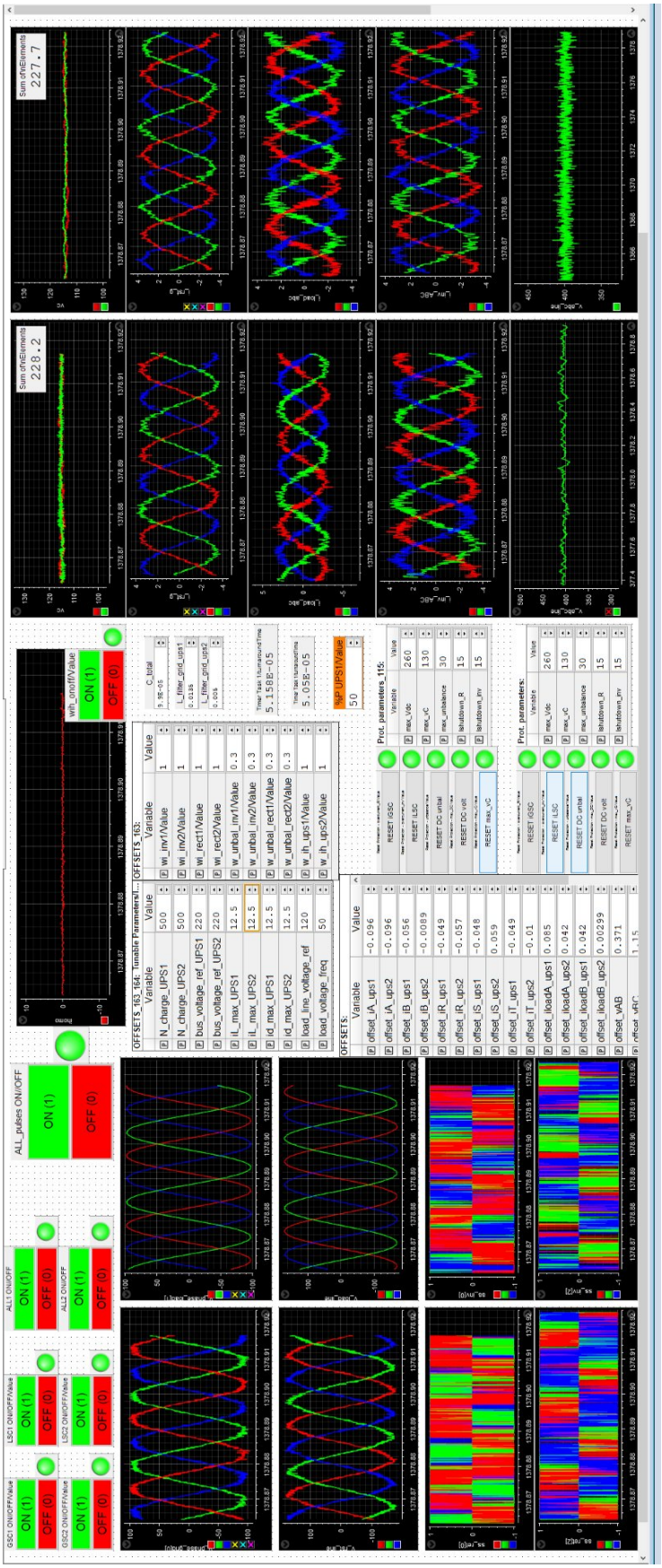


Figure B.18: Developed monitoring and control panel in *ControlDesk*.

Figure B.19: Autotransfomer.

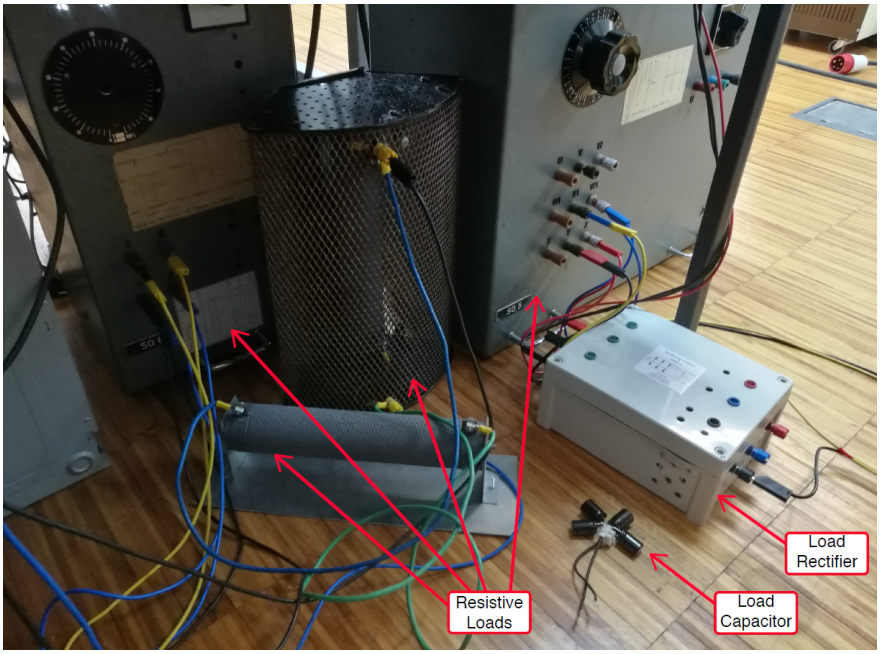



Figure B.20: Loads used in the experimental tests.

# Appendix C

# Submitted and Accepted Paper

This appendix presents a paper that resulted from part of the work done during this dissertation. The paper, with the title "Load-sharing between two paralleled UPS systems using Model Predictive Control" was submitted to the 45th Annual Conference of the IEEE Industrial Electronics Society (IECON 2019), and accepted. The conference will occur in Lisbon on October 14-17, 2019.

# Load-sharing between two paralleled UPS systems using Model Predictive Control

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***Abstract*—Increasing the power rating and reliability of a power conversion system are the main reasons for the parallel operation of power electronics converters. However, when linked in parallel, the converters are subjected to a circulating current that compromises optimum system operation. Moreover, due to efficiency and flexibility reasons, a strategy for power-sharing is crucial. This paper proposes a Finite Control Set Model Predictive Control (FCS-MPC) scheme for two parallel connected Uninterruptible Power Supply (UPS) systems based on two 3-Level Neutral Point Clamped (3LNPC) converters. With the proposed control scheme, a precise load-sharing can be defined, with different power being supplied by each UPS system. Simultaneously, the Zero Sequence Circulating Current (ZSCC) can be effectively suppressed. Simulation results validate the proposed control scheme.**

## I. Introduction

The use of paralleled power electronics converters is getting more and more popular as a way to improve system power rating, efficiency and reliability. When converters are paralleled, two big concerns arise: potential circulating current must be suppressed and load current must be distributed among systems according to their availability.

Since the inputs/outputs of each converter are connected a path for the circulation of a zero sequence current can be formed. The ZSCC is generated by asymmetries in converters' control and circuit parameters [1]. The ZSCC distorts input and output currents of the systems, increases power losses [2] and hinders precise load-sharing between paralleled systems. Some studies have been proposed to suppress the ZSCC in 3-level voltage source inverters (VSIs) that share the same DC and AC buses [3, 4]. Multilevel converters have a lot of advantages when compared to the conventional 2-level converters [5]. As the number of levels in output voltage increases, lower voltage and current distortion is produced as well as lower switching losses. Due to DC bus voltage distribution through a high number of semiconductors, higher voltage ratings can also be achieved. In that way, 3LNPC have been object of intense research in the last few decades as well as their use in back-to-back (BTB) topologies [6, 7, 8].

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The most common strategies for ZSCC suppression are based on passive, control, and modulation methods [3]. The use of passive methods, such as the adoption of transformers and common mode inductors are not viable for some applications, since system weight and cost are increased. When compared to modulation based control techniques, the FCS-MPC concept is more simple and intuitive. Moreover, this type of control presents faster dynamic response and allows an easy inclusion of non-linearities and constrains. Thus, strategies based on the FCS-MPC have been proposed for paralleled 3-Level VSIs. In [3, 4] strategies based on this type of control are proposed for 3-Level T-type grid-connected paralleled inverters. With the proposed schemes, the ZSCC is eliminated. Moreover, output power can be asymmetrically divided between the paralleled converters.

Regarding strategies for paralleled BTB systems control, in [9] a control scheme for two BTB systems that drive a Permanent Magnet Synchronous Motor (PMSM) is proposed. The ZSCC can be effectively eliminated without additional passive elements. In [10] the use of multiple parallel connected BTB systems in a Doubly-Fed Induction Machine (DFIM) is studied. Each BTB system is based on two 3LNPC. In this case, the ZSCC is avoided using interphase reactors, which increases system weight, size and cost. In both studies, the total output current is symmetrically divided between the paralleled converters.

Asymmetric load power distribution is crucial due to efficiency and reliability reasons. The efficiency of a power conversion system increases with the load. When a power electronic converter operates at low load, power losses become more significant, leading to low efficiency values. Therefore, in paralleled converters, an asymmetric power distribution can increase the overall system efficiency. Moreover, if one converter is not able to supply its power target (for example due to a fault), then the other converters must increase their target power, to maintain the system correct operation.

The main controller priority of a UPS system is to generate a high-quality output voltage waveform. Therefore, output voltage is usually directly controlled in FCS-MPC. When two UPS systems are paralleled, controlling the output voltage directly, does not allow a direct load-sharing control.

Hence, this paper proposes a strategy that allows asymmetric distribution of the load power between two paralleled UPS

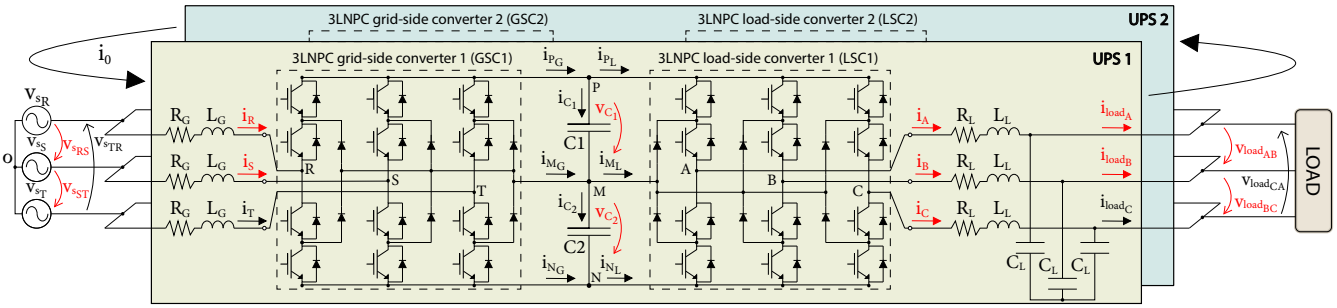


Figure 1. Circuit diagram of the proposed parallel system

systems and ZSCC suppression. With the proposed control scheme, the output currents are directly controlled, ensuring asymmetric power distribution between UPSs and simultaneously a high quality voltage waveform. This paper is organized as follows: in section II, the mathematical model of the UPS system and the dynamics of ZSCC are presented. In section III, the discretized model equations and the principles of FCS-MPC are demonstrated. In section IV, simulation results are presented. Section V concludes the paper.

## II. Studied System and Mathematical Model

Fig. 1 illustrates the adopted system topology. The measured signals are represented in red. Each UPS system contains a grid-side converter (GSC) and a load-side converter (LSC) that share a double capacitor DC bus. Since the UPS batteries and the DC-DC converter do not have any influence in the ZSCC circulation, they are not considered. The GSCs are connected to the grid using an inductive filter while the LSCs are connected to the load through an LC filter. The paralleled systems are symmetric, which means that their circuit configuration and parameters are the same. The adopted 3LNPC topology contains 3 legs, each of them associated to a given phase $X$. For the GSC $X = \{R, S, T\}$, whereas for the LSC $X = \{A, B, C\}$. Each leg contains 4 IGBT (with anti-parallel diodes), and 2 clamping diodes. For each phase there are three distinct switching states $S_X \in \{1, 0, -1\}$, leading to three different pole voltage values $v_{XM} \in \{v_{C1}, 0, -v_{C2}\}$, respectively. Therefore, the 3LNPC converter has 27 possible switching states. The pole voltage $v_{XM}$ corresponds to the voltage between the AC terminal of phase $X$ and the middle point $M$ of the DC bus. To simplify the control of each converter, 3-phase variables are transformed to space vector form. Regarding the GSC, such transformation is given by

$$\overline{x} = \frac{2}{3}(x_R + a x_S + a^2 x_T) = x_\alpha + j x_\beta \,, \tag{1}$$

where $a = e^{j\frac{2\pi}{3}}$ represents the space rotation coefficient and $\overline{x}$ represents the space vector. The LSC variables are transformed analogously.

### A. Grid-side converter

The inductive filter that connects the GSC AC side to the grid was chosen to ensure appropriated current filtering without compromising the dynamic response of the converter. The GSC DC side is connected to the DC bus. The following voltage equation can be written

$$v_{s_X} = L_G \frac{di_X}{dt} + R_G i_X + v_{XM} - v_{OM} \,. \tag{2}$$

The term $v_{s_X}$ corresponds to the grid phase voltage which is calculated from the measured line voltages. The term $v_{OM}$ corresponds to the converter Common Mode Voltage (CMV). The CMV is deduced from (2), and is given by

$$v_{OM} = \frac{v_{RM} + v_{SM} + v_{TM}}{3} \,. \tag{3}$$

All three-phase signals are transformed to vector form. This removes the CMV component, simplifying the converter control. Therefore, equation (2) can be rewritten as

$$\overline{v}_s = L_G \frac{d\overline{i}_g}{dt} + R_G \overline{i}_g + \overline{v}_g \,. \tag{4}$$

From (4), the dynamics of the grid-side current is given by

$$\frac{d\overline{i}_g}{dt} = \frac{\overline{v}_s}{L_G} - \frac{R_G}{L_G}\overline{i}_g - \frac{\overline{v}_g}{L_G} \,. \tag{5}$$

The dynamics of DC bus capacitors voltage are defined as

$$\frac{dv_{C1}}{dt} = \frac{1}{C_{DC}} i_{C1} \,, \quad \frac{dv_{C2}}{dt} = \frac{1}{C_{DC}} i_{C2} \,, \tag{6}$$

where the currents in capacitors $C1$ and $C2$ are respectively given by $i_{C1} = i_{P_G} - i_{P_L}$ and $i_{C2} = i_{N_L} - i_{N_G}$. In these equations, $i_{P_G}$ and $i_{N_G}$ are the currents supplied to the DC bus by the GSC, whereas $i_{P_L}$ and $i_{N_L}$ are the currents absorbed by the LSC. The currents absorbed by the DC bus are given by

$$\begin{aligned} i_{P_G} &= i_R\ (S_R = 1) + i_S\ (S_S = 1) + i_T\ (S_T = 1) \\ i_{M_G} &= i_R\ (S_R = 0) + i_S\ (S_S = 0) + i_T\ (S_T = 0) \\ i_{N_G} &= i_R\ (S_R = \text{-}1) + i_S\ (S_S = \text{-}1) + i_T\ (S_T = \text{-}1) \,, \end{aligned} \tag{7}$$

where $(S_X = s)$ is 1 if $S_X$ has value $s$ and 0 otherwise. The currents $i_{P_L}$, $i_{M_L}$ and $i_{N_L}$ are obtained analogously. The capacitance of each DC bus capacitor is the same, whereby $C1 = C2 = C_{DC}$.

### B. Load-side converter

The LSC DC side is connected to the DC bus, whereas the AC side is connected to the load through an LC filter that ensures high quality in output voltage waveform. Similarly to the mathematical model deduction made for the GSC, the following phase voltage equation can be written for the LSC

$$v_{load_X} = -L_L \frac{di_X}{dt} - R_L i_X + v_{XM} - v_{O'M} \ , \qquad (8)$$

where the term $v_{load_X}$ is the load phase voltage which is calculated from the measured line voltages. The term $i_X$ is the LSC output current. The terms $v_{XM}$ and $v_{O'M}$ are respectively the pole voltage and CMV of the LSC, being O' in this case a fictitious neutral load point. The current equations are given by

$$i_X = i_{load_X} + i_{C_{L_X}} = i_{load_X} + C_L \frac{dv_{load_X}}{dt} \ . \qquad (9)$$

In vector form, (8) and (9) are given respectively by

$$\overline{v}_{load} = -L_L \frac{d\bar{i}_L}{dt} - R_L \bar{i}_L + \overline{v}_L \ , \qquad (10)$$

$$\bar{i}_L = \bar{i}_{load} + C_L \frac{d\overline{v}_{load}}{dt} \ . \qquad (11)$$

Hence, the voltage and current dynamics are given by

$$\frac{d\bar{i}_L}{dt} = -\frac{1}{L_L}\overline{v}_{load} - \frac{R_L}{L_L}\bar{i}_L + \frac{1}{L_L}\overline{v}_L \ , \qquad (12)$$

$$\frac{d\overline{v}_{load}}{dt} = \frac{1}{C_L}\bar{i}_L - \frac{1}{C_L}\bar{i}_{load} \qquad (13)$$

### C. Analysis of the ZSCC in paralleled UPS systems

The ZSCC that circulates between the UPS systems through the connection points, can be directly calculated by summing the phase currents at any point of the paralleled system. Therefore, all the LSC1 output currents of the UPS1 are measured. The ZSCC is given by

$$i_0 = \frac{i_A + i_B + i_C}{3} \ . \qquad (14)$$

Similarly to the ZSCC dynamics analysis given in [3] for the parallel of two 3-Level T-type inverters, the following equation is deduced to study the dynamics of ZSCC in the studied paralleled UPS systems

$$\frac{di_0}{dt} = \frac{3}{2} \cdot \frac{(v_{OM_{G2}} - v_{O'M_{L2}} + v_{O'M_{L1}} - v_{OM_{G1}})}{(R_G + R_L + L_G + L_L)} \ , \qquad (15)$$

where $v_{OM_{G2}}$, $v_{O'M_{L2}}$, $v_{O'M_{L1}}$, $v_{OM_{G1}}$ are the CMV of each converter, calculated using (3). The chosen convention for the positive direction of ZSCC is depicted in Fig. 1. From (15) it can be seen that ZSCC dynamics highly depends on the linear combination of CMV of all the converters. Thus, by controlling the CMV generated by the converters, the ZSCC can be suppressed.

## III. Proposed FCS-MPC controller

The control principle is the same for the two paralleled systems. Therefore, the control scheme explained in this section is valid for both UPSs. Each UPS system is controlled by an independent control platform. This means that the controller of UPS1 will send signals to the IGBTs of LSC1 and GSC1, and the same is applied for the UPS2. As proposed in [11], a cooperative control strategy is adopted. The control action regarding the LSC is the first to be calculated. This means that the LSC switching state is chosen having in account only its effect in the respective UPS system. However, to choose the switching state to apply on the GSC, the controller takes into account the switching state already chosen for the LSC.

### A. Controller delay compensation

In spite of the remarkable increase in processing capabilities of digital controllers, it is still impossible to acquire data, process it and output control decision almost instantaneously. Therefore, as used in [11], a delay of one sample is considered between signal measurement and the corresponding control action. All required signals are measured at $k$. Then, system state at $k+1$ is predicted, considering the previously chosen control action (applied at $k$). Finally the system state at $k+2$ is predicted for all possible switching states and the one that minimizes the cost function is selected and applied at $k+1$.

In order to discretize the model, the forward Euler approximation is used. Hence, from the mathematical model previously presented, the system state at $k+1$ is predicted using the following equations

$$\overline{v}_s^p[k+1] = \overline{v}_s[k] \cdot e^{\frac{2\pi}{0.02}Ts} \qquad (16)$$

$$\bar{i}_g^p[k+1] = \left(1 - \frac{R_G T_s}{L_G}\right)\bar{i}_g[k] + \frac{T_s}{L_G}\overline{v}_s[k] - \frac{T_s}{L_G}\overline{v}_g[k] \qquad (17)$$

$$i_0^p[k+1] = i_0[k] + \frac{3T_s(v_{OM_{G2}} - v_{O'M_{L2}} + v_{O'M_{L1}} - v_{OM_{G1}})[k]}{2(R_G + R_L + L_G + L_L)} \qquad (18)$$

$$v_{C_n}^p[k+1] = v_{C_n}[k] + \frac{T_s}{C_{DC}} i_{C_n}[k] \ , \ \ n = \{1, 2\} \qquad (19)$$

$$\overline{v}_{load}^p[k+1] = \overline{v}_{load}[k] + \frac{T_s}{C_{eq}}(\bar{i}_{C_{L_{(UPS1)}}}[k] + \bar{i}_{C_{L_{(UPS2)}}}[k]) \qquad (20)$$

$$\bar{i}_L[k+1] = \left(1 - \tfrac{R_L T_s}{L_L}\right)\bar{i}_L[k] - \tfrac{T_s}{L_L}\overline{v}_{load}[k] + \tfrac{T_s}{L_L}\overline{v}_L[k]. \qquad (21)$$

where $T_s$ is the sampling time and $C_{eq}$ is the equivalent filter capacitance.

### B. Load-sharing control strategy

Since both UPS systems are sharing the same load, each control platform must know the total load current. This means that the output load current being supplied by UPS1 is sent to the control platform of UPS2, and vice versa. Independently of the power distribution between systems, load voltage must follow a sinusoidal voltage reference. Since a direct control of the load voltage does not allow a load-sharing strategy, this voltage is controlled through a control scheme based on direct

current control. An equivalent output capacitor filter is defined as $C_{eq} = 2 \cdot C_L$. The total current flowing in $C_{eq}$ is controlled, so that the load voltage follows the voltage reference. The percentage of power that each system supplies to the load is defined by controlling the current that each system injects in $C_{eq}$. The proportion of load power assigned to UPS1 is defined as $\lambda_1$, whereby the proportion of power supplied by UPS2 is given by $\lambda_2 = 1 - \lambda_1$. Using the backward Euler approach, the total current necessary in the equivalent capacitor to track the output voltage reference is given by

$$\overline{i}^*_{L_T}[k+2] = \overline{i}_{load_T}[k+2] + \frac{C}{T_s}(\overline{v}^*_{load}[k+2] - \overline{v}^p_{load}[k+1]) \,, \tag{22}$$

where $\overline{i}^*_{L_T}[k+2]$ is the reference current vector, $\overline{v}^*_c[k+2]$ is the reference voltage vector and $\overline{i}_{load_T}[k+2]$ the total load current. Finally, the current references for each UPS system are given by

$$\overline{i}^*_{L1}[k+2] = \lambda_1 \cdot \overline{i}^*_{L_T}[k+2], \tag{23}$$

$$\overline{i}^*_{L2}[k+2] = \lambda_2 \cdot \overline{i}^*_{L_T}[k+2]. \tag{24}$$

### C. Grid-side currents references calculation

The developed control scheme for GSC control is based on the conventional control strategy presented in [11]. The grid current reference calculation is based on active power balancing in each UPS. The power balancing in one system can be written as

$$P^*_{grid} = (P_{grid} - P_G) + P_L + P^*_{charge} \,, \tag{25}$$

where, $P^*_{grid}$ corresponds to the reference active power to be drawn from the grid; $P_{grid}$ is the power actually drawn from the grid; $P_G$ is the power supplied by the grid-side converter to the DC bus; $P_L$ is the power drawn from DC bus by the LSC. The difference $P_{grid} - P_G$ represents the losses in the GSC. Finally, the term $P^*_{charge}$ corresponds to the power necessary to charge/discharge the DC bus to the reference voltage value. To calculate this term the following equation is used

$$P^*_{charge} = \frac{C_{DC} \cdot (v^{*2}_{DC} - v^2_{DC})}{4 \cdot T_s \cdot N_{th}} \,, \tag{26}$$

where $C_{DC}$ represents the capacitance of one DC bus capacitors. The term $v^*_{DC}$ is the DC bus voltage reference and $v_{DC}$ is the measured bus voltage. To limit the currents drawn by the GSC, a time horizon of $N_{th}$ samples is adopted.

The grid current references are calculated using the following equation:

$$\overline{i}^*_g[k+2] = \frac{2}{3} \cdot \left( \frac{P^*_{grid}}{|\overline{v}_s|} + j\frac{Q^*_{grid}}{|\overline{v}_s|} \right) \cdot e^{j(\angle \overline{v}_s + 2\pi \frac{2T_s}{0.02})} \,, \tag{27}$$

where $Q^*_{grid}$ is the target reactive power to be absorbed from grid. Usually, this term is desired to be null, however in specific cases, as for PF correction, it can be regulated into a certain value. The amplitude and phase of grid voltage vector ($|\overline{v}_s|$ and $\angle \overline{v}_s$) are obtained using a Phase-Locked Loop (PLL). The constant $2\pi \frac{2T_s}{0.02}$ is added to $\angle \overline{v}_s$ in order to obtain the reference currents at $k+2$.

### D. Load-side controller

Three objectives are considered regarding the LSC control:

1) Converter output current error minimization;
2) Minimization of DC bus capacitors voltage unbalance;
3) Minimization of the ZSCC.

The predicted output converter current at $k+2$ is given by

$$\overline{i}^p_L[k+2] = \overline{i}^p_L[k+1] - \frac{T_s}{L_L}\overline{v}^p_{load}[k+1] - \frac{T_s R_L}{L_L}\overline{i}^p_L[k+1] + \frac{T_s}{L_L}\overline{v}_L[k+1] \tag{28}$$

where $\overline{v}_L[k+1]$ corresponds to the converter voltage vector at $k+1$. This is the only variable term in the equation since it depends on the switching states being evaluated to be applied at $k+1$.

Due to limitations in real-time communication between independent control platforms of both UPSs, each controller only knows the switching states to be applied at $k+1$ in the converters of the respective UPS. The predicted ZSCC considered by control platforms of UPS1 and UPS2 when computing control action for the respective LSCs are given by

$$i^p_{0_{L1}}[k+2] = i^p_0[k+1] + \frac{3T_s(v_{O'M_{L1}}[k+1])}{2(L_G + L_L + R_G + R_L)} \,, \tag{29}$$

$$i^p_{0_{L2}}[k+2] = i^p_0[k+1] + \frac{3T_s(-v_{O'M_{L2}}[k+1])}{2(L_G + L_L + R_G + R_L)} \,. \tag{30}$$

The DC bus capacitors unbalance at $k+2$ is given by:

$$\Delta v^p_{C_{1,2}}[k+2] = \Delta v^p_{C_{1,2}}[k+1] + \frac{T_s}{C_{DC}} i_{M_L}[k+1] \,, \tag{31}$$

where $\Delta v^p_{C_{1,2}} = v^p_{C1} - v^p_{C2}$.

The partial objective functions regarding output current, DC bus capacitors unbalance and ZSCC are respectively given by

$$g_{i_L} = \sqrt{(i^*_{L_\alpha}[k+2] - i^p_{L_\alpha}[k+2])^2 + (i^*_{L_\beta}[k+2] - i^p_{L_\beta}[k+2])^2} \tag{32}$$

$$g_{bal_L} = |v^p_{C1}[k+2] - v^p_{C2}[k+2]| \tag{33}$$

$$g_{z_L} = |i^p_{0_L}[k+2]| \tag{34}$$

The objective function regarding LSC control is given by

$$G_{LSC} = g_{i_L} \cdot W_{i_L} + g_{bal_L} \cdot W_{bal_L} + g_{z_L} \cdot W_{z_L}. \tag{35}$$

This equation is evaluated for the 27 possible combinations, and combines partial objective functions $g_x$ weighted by respective weight $W_x$, associated with each of the three objectives.

### E. Grid-side controller

Regarding the GSC control, three objectives are also considered:

1) Reference grid current vector tracking;
2) Minimization of DC bus capacitors voltage unbalance;
3) Minimization of the ZSCC.

After the LSC controller is computed, the GSC objective function at $k+2$ can be evaluated. The predicted grid current vector is given by

$$\overline{i}_g^p[k+2] = \overline{i}_g^p[k+1] - \frac{R_G T_s}{L_G}\overline{i}_g^p[k+1] + \frac{T_s}{L_G}\overline{v}_s^p[k+1] - \frac{T_s}{L_G}\overline{v}_g[k+1]\,. \tag{36}$$

The predicted DC bus capacitor unbalance is given by

$$\Delta v_{C_{1,2}}^p[k+2] = \Delta v_{C_{1,2}}^p[k+1] + \frac{T_s}{C_{DC}}\left(i_{M_L}[k+1] - i_{M_G}[k+1]\right)\,. \tag{37}$$

The predicted ZSCC considered by each control platform to select the control action for the GSCs are given by

$$i_{0_{G1}}^p[k+2] = i_0^p[k+1] + \frac{3T_s(v_{O'M_{L1}}[k+1] - v_{OM_{G1}}[k+1])}{2(L_G + L_L + R_G + R_L)}, \tag{38}$$

$$i_{0_{G2}}^p[k+2] = i_0^p[k+1] + \frac{3T_s(v_{OM_{G2}}[k+1] - v_{O'M_{L2}}[k+1])}{2(L_G + L_L + R_G + R_L)}. \tag{39}$$

Since the control action to be taken by the LSC was already selected, its effect is also taken into account ($v_{O'M_{L1}}$,$v_{O'M_{L2}}$). Finally, the objective function regarding GSC control is

$$G_{GSC} = g_{i_G}\cdot W_{i_G} + g_{bal_G}\cdot W_{bal_G} + g_{z_G}\cdot W_{z_G}\,. \tag{40}$$

where the terms $g_{i_G}$, $g_{bal_G}$ and $g_{z_G}$ are calculated analogously to (32), (33) and (34), respectively.

## IV. Simulation Results

The proposed control scheme for ZSCC reduction and load-sharing in paralleled UPS systems is tested using *Matlab/Simulink*. An RMS line voltage of 120 V is considered for the grid and UPS output. Each GSC is connected to the power grid through an inductance of 5 mH. The load side filters have an inductance of 2.7 mH and capacitance value of 66 $\mu$F. The DC bus voltage reference is 220 V. The DC bus contains two capacitors of 8.2 mF. A sampling time of 70 $\mu$s is used.

Fig. 2 shows the effectiveness of control scheme in reducing the ZSCC, when the UPS1 is supplying 75 % of load power, and the UPS2 is supplying the remaining 25% ($\lambda_1 = 0.75$). The system is feeding a 10 $\Omega$ linear load. Until $t = 0.05$ s, the ZSCC suppression is activated ($W_{z_G} = W_{z_L} = 0.1$). After that instant, the ZSCC suppression is deactivated ($W_{z_G} = W_{z_L} = 0$). After this, a circulating current immediately appears reaching values of almost 5 A. Consequently, the currents becomes highly distorted, especially in the UPS that is supplying less power. It is worth mentioning that the total grid and load currents aren't affected by the circulation of ZSCC. However, the THD of each UPS currents and power distribution between the UPS systems are compromised. At $t = 0.2$ s the ZSCC suppression is reactivated, and therefore ZSCC rapidly takes a negligible value, leading to practically sinusoidal input and output currents. A practically sinusoidal voltage waveform (THD=1.06 %) is obtained even when ZSCC isn't suppressed.

In Fig. 3 the response of the system during power distribution changes is demonstrated. Until $t = 0.1$ s the UPS1 is supplying 25 % of load power. At $t = 0.1$ s, a distribution of 50% is made. Finally, at $t = 0.2$ s, $\lambda_1$ is changed to 0.75. It can be seen from the output currents that the power supplied by each UPS changes immediately to the target value. A slower transition is observed in the displayed output average power simply because a time horizon of one period is considered in its calculation.

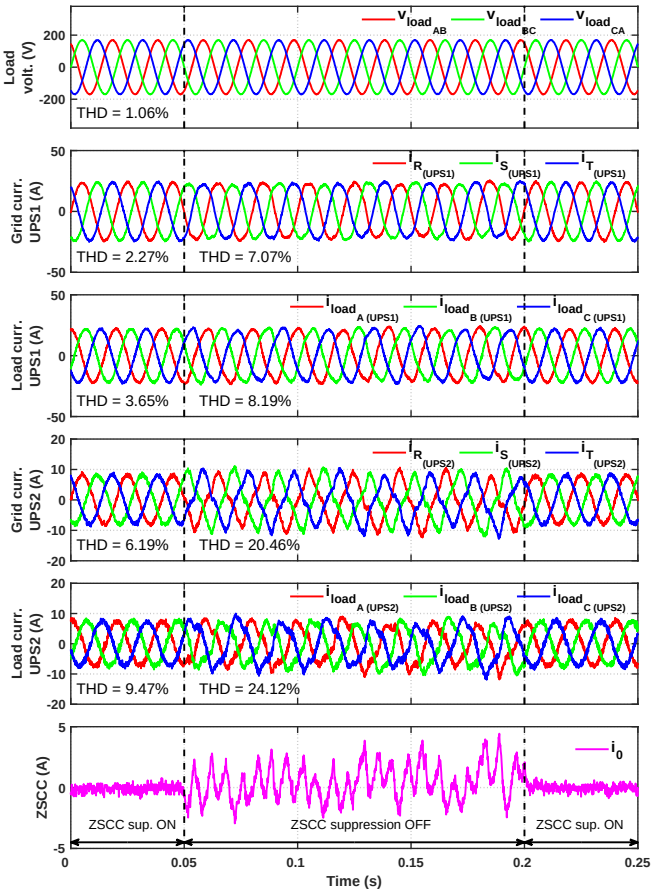


Figure 2. Grid and load currents when system is feeding a linear load w/ UPS1 supplying 75% of load power ($W_{i_G} = W_{i_L} = 1, W_{bal_G} = W_{bal_L} = 0.3$).

To demonstrate the system operation when supplying a highly non-linear load, a three-phase diode rectifier feeding an RC parallel circuit (R=10 $\Omega$; C=157 $\mu$F) is used. The UPS systems are subjected to the same power variations of the previous case. As shown in Fig. 4, even when supplying a non-linear load, and simultaneously changing load power distribution, high quality output voltage waveform is obtained (THD = 4.65 %). The DC bus capacitors voltage balance is also ensured. Moreover, Fig. 4 demonstrates the fast DC bus voltage tracking in both UPS systems. These results demonstrate the robustness of the proposed control scheme for asymmetric load-sharing operation.

## V. Conclusion

In this paper, an FCS-MPC control scheme for the parallel operation of two UPS systems is proposed. The proposed control scheme allows asymmetric load power distribution between systems as well as ZSCC current suppression. Simulation results show good dynamic response and steady-state

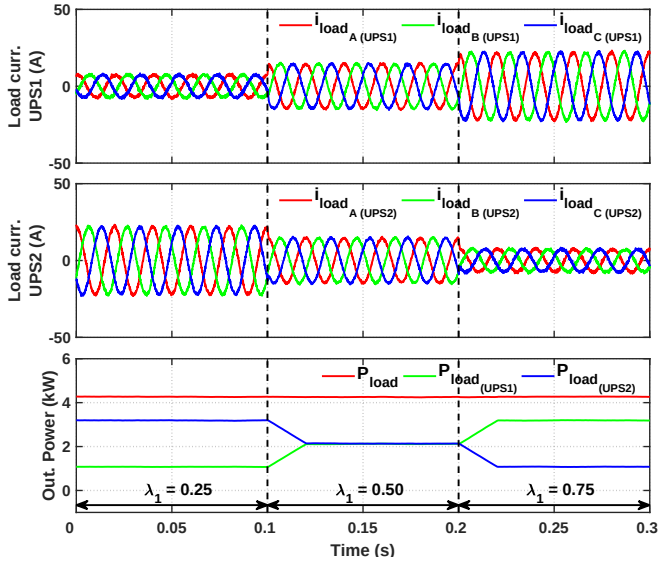


Figure 3. System operation when different percentage of power is assigned to each UPS system ($W_{i_G} = W_{i_L} = 1, W_{bal_G} = W_{bal_L} = 0.3, W_{z_G} = W_{z_L} = 0.1$).

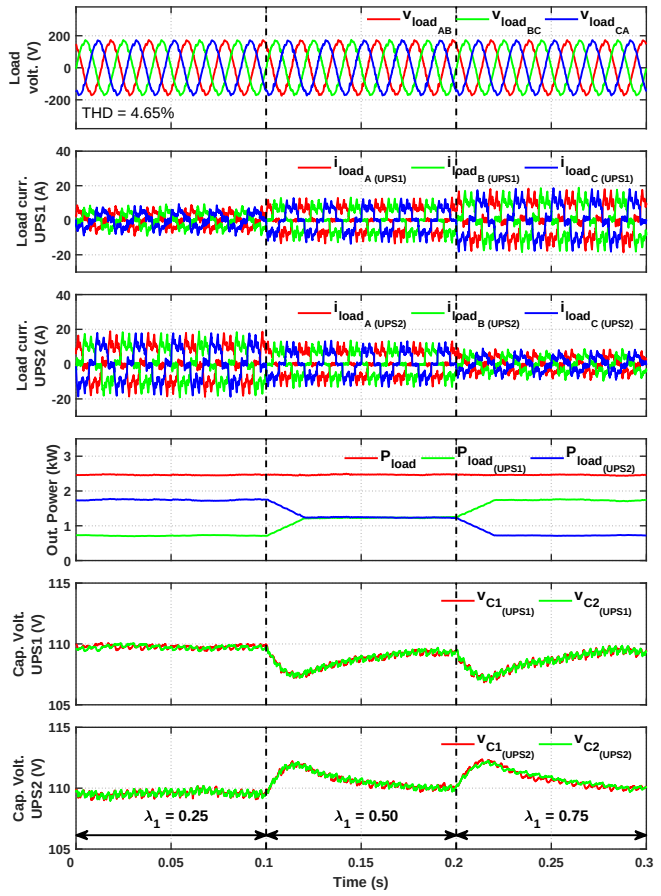


Figure 4. System operation when supplying a highly non-linear load ($W_{i_G} = W_{i_L} = 1, W_{bal_G} = W_{bal_L} = 0.3, W_{z_G} = W_{z_L} = 0.1$).

performance in different load-sharing conditions. Moreover, the system draws practically sinusoidal currents from the grid. Even though the output voltage is not controlled directly, high quality load voltage waveforms are obtained even with highly non-linear loads.

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